What Is a Thermoelectric Cooler?

How It Works · Its Characteristics · How to Design a TEC System with Optimized Performance

White Paper AW-TECM-01 · Rev. 2.4 · June 2026

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QUICK ANSWER

A thermoelectric cooler (TEC) is a solid-state bidirectional heat pump based on the Peltier effect. When DC current flows through its Bi_2Te_3 semiconductor couples, heat moves from one ceramic face to the other. Reversing the current instantly switches between cooling below ambient and heating above it.

Select a module with Qmax about 4–6× the real cooling load for balanced precision work and operate at 20–35% of Imax (see §5.3 for the full oversizing table covering all design targets).

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Abstract

This white paper is a engineering reference for thermoelectric coolers (TECs), also known as Peltier modules. It explains the physics, construction, datasheet interpretation, selection, thermal-network design, controller selection, assembly, reliability, and application of TEC modules — from first principles through advanced theory — using rigorous equations, intuitive analogies, engineering illustrations and a normalized performance-curve library, and three fully worked design examples. All design examples use the Analog Technologies (ATI) ATE1-127 series of single-stage TEC modules and ATI precision TEC controllers. Whether you are stabilizing a DFB laser wavelength to ±0.001 nm, cooling a CCD sensor 45 °C below ambient, or managing a 40 W localized hotspot on an AI accelerator, this document gives you the engineering framework, equations, and examples needed to design, build, and deploy a working TEC thermal-management system. For product specifications and ordering, visit www.analogtechnologies.com.

Keywords: *thermoelectric cooler, TEC module, Peltier module, Peltier cooler, thermoelectric cooling, TEC controller, Peltier effect, Seebeck effect, solid-state cooling, precision temperature control, heat pump, thermal management, TEC design guide, TEC selection, COP, ΔT_{max}, Qmax, ZT, figure of merit, heat sink sizing, laser diode cooling, CCD cooling, AI chip cooling, hotspot cooling, the ATE1-127 series, bismuth telluride.* See the complete ATE1-127 series product page for specifications and ordering.

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Nomenclature

Note: Temperatures (Tc, Th, Tamb) must be in Kelvin (K) when they appear inside a Peltier term (α·T·I) or the Z formula. Temperature differences (ΔT, ΔTmax) have the same numerical value in K and °C and may be substituted freely.

The following symbols and abbreviations are used throughout this white paper. All temperatures may be expressed in either Kelvin (K) or degrees Celsius (°C) as indicated by context; temperature *differences* (ΔT) are numerically identical in both scales.

Symbol	Definition	Units

TEC	Thermoelectric cooler (Peltier module)	—
Z	Thermoelectric figure of merit; $Z = \alpha^2/(R \cdot K) = 2 \cdot \Delta T_{max}/T_{c,ref}^2$, where $T_{c,ref} = T_{h,ref} - \Delta T_{max}$	K^{-1}
Q_c	Heat absorbed at the cold surface (cooling power)	W
Q_h	Heat rejected at the hot surface	W
Q_{max}	Maximum cooling capacity (at $\Delta T = 0$, $I = I_{max}$)	W
Pin	TEC electrical power consumption ($V \cdot I$)	W
T_h	Hot-side (substrate) temperature	K or °C
T_c	Cold-side (device) temperature	K or °C
T_{amb}	Ambient temperature	K or °C
ΔT	Temperature difference across the TEC ($T_h - T_c$)	K or °C
ΔT_{max}	Maximum achievable ΔT (at $Q_c = 0$, $I = I_{max}$)	°C
I	Operating current through the TEC module	A
I_{max}	Maximum rated current (produces ΔT_{max} at $Q_c = 0$)	A
I_{opt}	Optimum current for maximum COP	A
V	Voltage across the TEC module	V
V_{max}	Maximum rated voltage (at I_{max}, ΔT_{max})	V
N	Number of thermoelectric couples (pellet pairs)	—
G	Pellet geometry factor (cross-section area / length)	cm
S_M	Module effective Seebeck coefficient (= V_{max} / $T_{h,ref}$)	V/K
R_M	Module effective electrical resistance	Ω
K_M	Module effective thermal conductance	W/K
s	Seebeck coefficient (material level, per thermoelectric leg/element)	V/K
k	Thermal conductivity (material level)	W/(cm·K)
ρ	Electrical resistivity (material level)	Ω·cm
COP	Coefficient of performance (Q_c / P_{in})	—
COP_{max}	Maximum COP at optimum current	—
R_{hs}	Heat-sink thermal resistance (hot side to ambient)	°C/W
R_{TIM}	Thermal interface material resistance	°C/W

K	Module thermal conductance (K ≡ KM); used in all system equations. W/K	W/K
R	Module electrical resistance (R ≡ RM); used in all system equations. Ω	Ω
α	Module Seebeck coefficient (α ≡ SM); used in all system equations. V/K	V/K
γ	Ioffe parameter = √(1 + Z·T̄), dimensionless	—
θ	Normalized temperature lift = ΔT / ΔTmax	—
$\bar{T}$	Mean absolute temperature = (Th + Tc) / 2	K
QPeltier,c	Peltier heat absorbed at cold side; = α·Tc·I	W
QJoule	Total Joule heat generated inside TEC; = $R \cdot I^2$	W
QJoule,c	Cold-side share of Joule heat; QJoule,c = ½·$R \cdot I^2$	W
QFourier	Fourier back-conduction heat leak; = K·ΔT	W
Th,ref	Datasheet reference hot-side temperature (typically 300 K)	K
Tc,ref	Cold-side temperature at ΔTmax condition; = Th,ref − ΔTmax	K

Sign convention: Positive current I is defined as conventional current entering the red (+) lead. Under ATI standard orientation, positive current cools the printed/model-number side. Reversing polarity reverses the heat-pumping direction.

Material-Level vs. Module-Level Properties

Thermoelectric analysis uses two distinct sets of transport properties that are often confused. Understanding the difference is essential for correctly interpreting datasheets and applying the performance equations in this paper.

Material-level properties (lowercase: s, k, ρ) describe the intrinsic behavior of the thermoelectric semiconductor material itself — typically bismuth telluride (Bi_2Te_3) alloyed with antimony or selenium. These are measured on a single pellet or bulk sample:

• s (Seebeck coefficient, V/K): the voltage generated per degree of temperature difference across one thermoelectric leg or element. Typical value for Bi_2Te_3 at 300 K: ≈ 200 μV/K per element, or ≈ 400 μV/K per N–P couple.

• k (thermal conductivity, W/(cm·K)): how readily the pellet material conducts heat by phonons and electrons. Lower is better for thermoelectric performance. Typical: 0.015 W/(cm·K).

• ρ (electrical resistivity, Ω·cm): the material's resistance to current flow. Lower is better (less Joule heating). Typical: 1.0×10^{-3} Ω·cm.

Module-level effective properties (uppercase with subscript M: S_M, K_M, R_M) describe the aggregate behavior of the entire assembled TEC module — all N couples wired in series electrically and arranged in parallel thermally, including solder joints, copper traces, and ceramic substrates. These are what the engineer actually uses in system-level calculations:

• S_M (module Seebeck coefficient, V/K) = V_{max} / T_h. This is the total Seebeck voltage of all N couples in series. Relationship to material: $S_M = 2N \cdot s$. For a 127-couple module with $s \approx 200$ µV/K: $S_M \approx 2 \times 127 \times 200$ µV/K ≈ 0.051 V/K.

• K_M (module thermal conductance, W/K): the rate at which heat leaks from hot to cold through the entire pellet array. Relationship to material: $K_M = 2N \cdot k \cdot G$, where G = (pellet cross-section area)/(pellet length). Note: higher K_M means more Fourier back-conduction loss.

• R_M (module electrical resistance, Ω): the total series resistance of all couples plus interconnects. Relationship to material: $R_M = 2N \cdot \rho / G$. This is what produces Joule self-heating ($\frac{1}{2} \cdot R_M \cdot I^2$).

Why the distinction matters. Material properties (s, k, ρ) are what physicists optimize when developing new thermoelectric compounds. Module properties (S_M, K_M, R_M) are what the thermal engineer needs for system design — and they can be computed directly from the four datasheet parameters (I_{max}, V_{max}, Q_{max}, ΔT_{max}) without knowing the internal pellet geometry or material composition. Section 5.2 of this paper derives all three module properties from these four datasheet values.

The module figure of merit Z ties everything together. It is defined identically at both levels:

Material level: $Z = s^2 / (\rho \cdot k)$

Module level: $Z = SM^2 / (RM \cdot KM) = 2 \cdot \Delta Tmax / (Th,ref - \Delta Tmax)^2 = 2 \cdot \Delta Tmax / Tc,ref^2$

Both expressions yield the same value (typically 2.4–2.7 × 10^{-3} K^{-1} for commercial Bi_2Te_3 modules at 300 K), confirming that the module-level derivation correctly captures the underlying material physics.

Symbol Convention: Throughout this paper, the symbols α, R, and K in the energy-balance equation $Qc = \alpha \cdot Tc \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$ refer to the MODULE-LEVEL effective properties (SM, RM, KM). They are NOT the single-pellet material values (s, k, ρ). The alias mapping is: $\alpha \equiv SM = 2N \cdot s$, $R \equiv RM = 2N \cdot \rho / G$, $K \equiv KM = 2N \cdot k \cdot G$. When you see α in an equation, think "total module Seebeck" not "material Seebeck per pellet." (The symbol ≡ means 'is identically equal to' or 'is defined as'.)

Design Workflow at a Glance: (1) Define Qc and ΔT from your thermal budget → (2) Select a module with Qmax ≥ 4–6× Qc → (3) Derive α, R, K from the datasheet bridge formulas → (4) Compute the operating point on normalized curves → (5) Size the heat sink for Qh = Qc + Pin → (6) Choose a controller and thermistor → (7) Assemble, test, and verify.

Sign convention: This equation is written for cooling mode, where positive current pumps heat from cold to hot and $\Delta T = Th - Tc > 0$. In equations containing $\alpha \cdot T \cdot I$, use absolute temperature in Kelvin.

PART I — FOUNDATION

What a TEC Is and How It Works

1. Introduction and Executive Summary

Scope: This paper focuses on single-stage Bi_2Te_3 TEC modules for room-temperature-class applications (−40 to +80 °C cold side), with notes on cascaded modules, H-series high-temperature variants, and emerging materials where relevant.

Temperature is not a background condition in precision engineering — it is a first-order design variable. Distributed-feedback (DFB) laser wavelength drifts at about 0.08 nm/°C; Fabry-Pérot laser diodes drift at 0.3 nm/°C. Dark current in CMOS and CCD image sensors approximately doubles every 6 to 8 °C. Quartz crystal references drift 0.1 to 1 ppm/°C. PCR reaction specificity collapses if the denaturation step misses 95 °C by more than ±0.5 °C. AI accelerator chips throttle when on-die hotspots exceed 105 °C. In every one of these cases, the difference between a product that works in the lab and one that works for ten years in the field is precise, active thermal management.

A thermoelectric cooler — also called a TEC module, Peltier module, or Peltier cooler — is a solid-state device that moves heat from one ceramic surface to another when DC current flows through it. It has no compressor, no refrigerant, no moving parts inside the cooling element, and no acoustic noise from the module itself (system noise depends on the heat-sink fan or liquid loop). It can

cool below ambient, heat above ambient, or stabilize at a precise setpoint — all by controlling the direction and magnitude of current.

This paper is organized in five parts that follow the engineer's natural workflow. Part I builds the foundation: Sections 1–4 give the physical picture and the energy balance, then Section 5 is a single comprehensive technical chapter that takes you all the way from datasheet reading through the normalized performance-curve library, advanced ΔT_{max} theory, and into hot-side thermal-network design. Part II turns that technical foundation into decisions — comparison with other cooling technologies, and the five-step module-selection flowchart. Part III is system design: the ATI ecosystem of controllers and accessories, and three fully worked examples spanning the design space. Part IV is everything that happens after the parts are ordered: mounting, common pitfalls, and reliability. Part V is context — applications, history, and the road ahead.

Quick answer: *A TEC is a solid-state heat pump that uses the Peltier effect to move heat through Bi_2Te_3 semiconductor couples, enabling silent, vibration-free, sub-ambient cooling with millikelvin precision.*

2. What Is a TEC? — The 30-Second Version

A thermoelectric cooler is a small, flat, solid-state device — typically 20 mm to 62 mm square and 3 to 5 mm thick — that pumps heat from one ceramic face to the other when you apply DC current. One face gets cold; the other gets hot. Reverse the current and the direction reverses. There is no compressor, no internal fan, no refrigerant gas, no moving parts.

One-sentence summary: A TEC is a solid-state heat pump that moves thermal energy from cold to hot using electricity — like a ferry carrying ice from one island to another.

The Heat-Ferry Analogy

Imagine two islands in a lake. The left island is your cold-side load — a laser diode, a detector, a PCR sample, or an AI chip. The right island is the heat sink, connected to the surrounding air or a liquid loop. Between them sails a cheerful ferry boat, the TEC, propelled by electrons.

Figure 1: The TEC island analogy. The Peltier ferry carries heat packets from the cold island to the hot island, while the electrical input adds Joule heat that must also be rejected on the hot side. The ferry's smokestack represents total Joule heating $Q_{Joule} = I^2R$. In the water, Fourier conduction $Q_{Fourier} = K \cdot \Delta T$ continuously leaks heat from the hot side back to the cold side, opposing the Peltier pumping.

The ferry picks up "ice balls" — packets of thermal energy — from the cold island and carries them to the hot island. But the ferry burns fuel to run its engine, and that fuel combustion (Joule heating from electrical power) also dumps heat onto the hot island. So the hot side receives the cargo heat AND the engine heat:

$$\mathbf{Qh = Qc + Pin}$$

This is the most important equation in TEC engineering. The heat sink must reject all of Qh — not just the useful cooling load Qc. Ignoring this rule is the thermal-engineering equivalent of asking a boat to carry cargo while pretending its engine produces no exhaust.

Meanwhile, heat leaks back from the hot island to the cold island through the water — the TEC body itself conducts heat in the wrong direction. The bigger the temperature difference, the faster the leak. At some point the ferry carries heat away as fast as it leaks back. That equilibrium defines ΔT_{max}, derived from first principles in Section 5.5.

Quick answer: *A TEC pumps heat with electrons; the hot side receives the cooling load plus the electrical input, and a Fourier leak through the TEC module body limits the achievable ΔT.*

3. Inside a TEC Module — Construction and Materials

Understanding what is physically inside a TEC module helps engineers make better decisions about handling, mounting, current limits, and failure modes. Modules look simple from outside — two flat ceramic plates with two wires — but the engineering inside the sandwich is dense.

3.1 The Semiconductor Couples

A TEC contains many thermoelectric couples: pairs of N-type and P-type bismuth telluride (Bi_2Te_3) semiconductor pellets connected electrically in series and thermally in parallel between two ceramic plates. Current flows through the N–P pellet chain, while heat flows through the pellet array from one ceramic face to the other.

The ATE1-127 series uses 127 couples per module, a common single-stage TEC architecture. The series places Vmax around 15.4 V, which is convenient for 12 V and 24 V system designs when used with a proper current-regulated TEC controller.

See the complete ATE1-127 series product page for specifications, mechanical drawings, thermal specifications, and selection guidance.

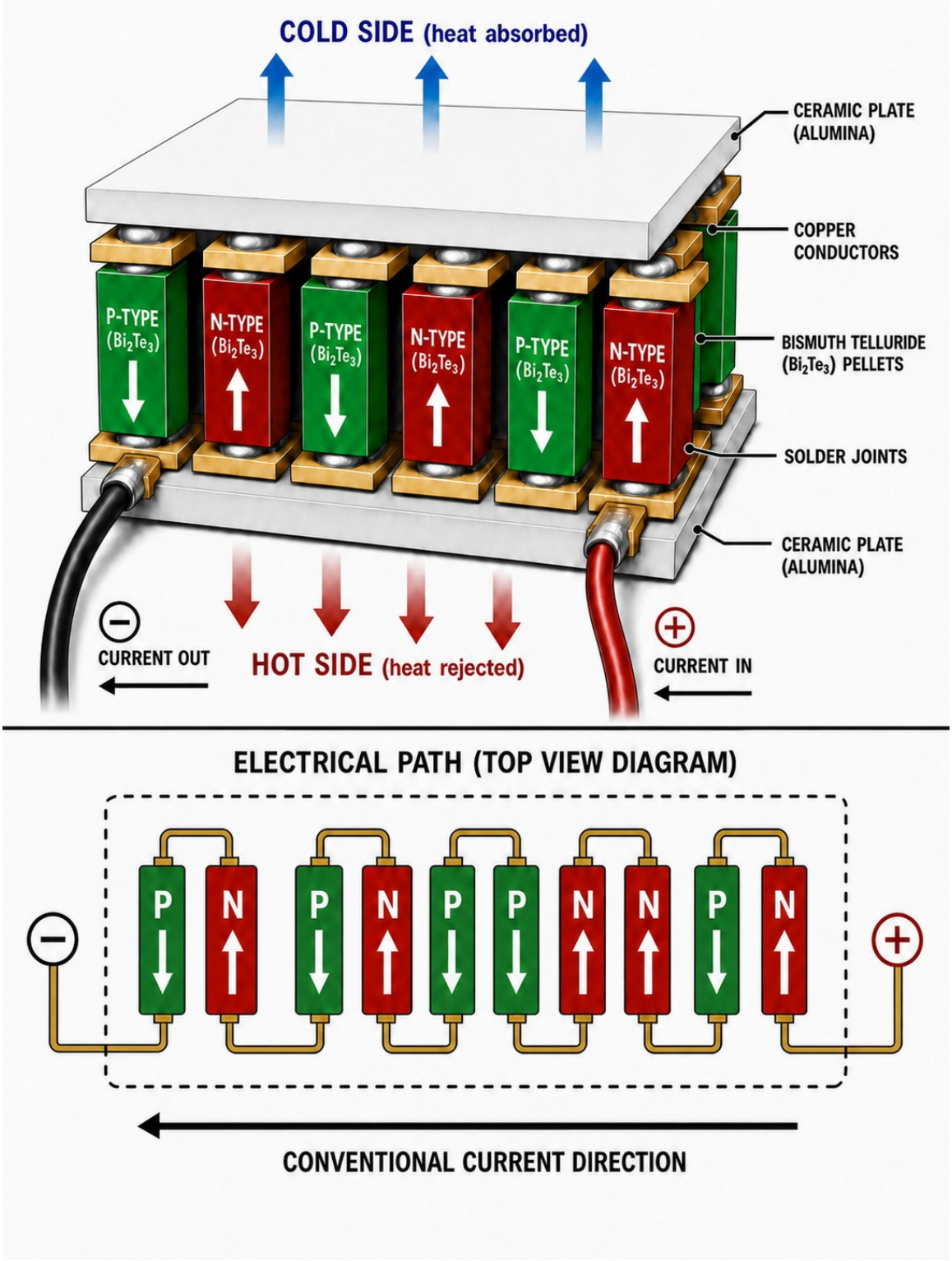

Figure 2: TEC module construction. For the standard red-positive cooling condition, the printed/model-number side is the cold side. The wire leads exit from the hot-side edge. Reversing current reverses the heat-pumping direction. Left: 3D cutaway showing N-type and P-type Bi_2Te_3 pellets between

ceramic substrates. Right: equivalent circuit with conventional current direction.

Each pellet is typically 1.0 to 1.4 mm square and 1.0 to 1.6 mm tall. Pellet aspect ratio (height to cross-section) is the primary geometric knob: tall thin pellets favor high ΔTmax with modest Qmax; short fat pellets favor high Qmax with modest ΔTmax. The ATE1-127 series uses geometries chosen to deliver 63 to 66 °C of ΔTmax across the ATE1-127 line.

3.2 The Ceramic Plates

The top and bottom surfaces are 96% alumina (Al_2O_3) ceramic — electrically insulating (preventing short circuits to the heat sink or device), thermally conductive (carrying heat across the full face), mechanically rigid (supporting the array against compression), and coefficient-of-thermal-expansion-matched to Bi_2Te_3 (minimizing thermal-cycling stress). For applications where every fraction of a degree matters, aluminum nitride (AlN) is available; AlN has 5 to 7× higher thermal conductivity than alumina.

3.3 The Solder System

Pellets are attached to copper interconnect traces using bismuth-tin (BiSn) solder for standard modules or tin-antimony (SnSb) solder for the H-series. Standard modules use BiSn with a 138 °C melting point and are rated for Th ≤ 85 °C (absolute maximum; engineering target is Th ≤ 50 °C for optimum lifetime and COP). H-series modules use SnSb (232 °C melting point) and support Th up to 200 °C — essential for automotive under-hood, industrial process control, and any application where the heat sink runs warm.

3.4 Wire Leads, Polarity, and Variants

Two insulated wire leads exit from the hot side: red (+) and black (−). Conventional current flows red-to-black to cool the labeled (cold) side; reversing polarity reverses the heat-pumping direction without damaging the module. The ATE1-127 series spans 49 variants: cooling capacity 20 to 252 W (at ΔT = 0), I_{max} 3 to 30 A, V_{max} 15.4 V across the line, three footprints (30×30, 40×40, 50×50 mm), open or sealed (S suffix), and standard or high-temperature (H suffix). This range covers a wide range of precision cooling applications from 1 W to 200 W without resorting to multi-stage stacking. Vmax stays nearly constant across the line because all variants share the same 127-couple architecture and Bi_2Te_3 chemistry; differences in cooling capacity (Qmax 20–252 W) come from the pellet geometry factor G, which scales R and K inversely while leaving α unchanged. See §5.2 for the closed-form bridge between datasheet specs and physical parameters.

Quick answer: *A TEC is a sandwich of N-P Bi_2Te_3 couples between two alumina ceramic plates; pellet geometry sets the ΔT_{max}-versus-Qmax tradeoff, and solder choice sets the maximum hot-side temperature.*

4. How a TEC Really Works — Math Meets Analogy

Section 2 gave you the 30-second version. Now we go deeper. A TEC exploits three thermoelectric effects simultaneously, and understanding their interplay is the key to every later decision — datasheet interpretation, selection, thermal-network sizing, and controller choice. For each effect we present both the rigorous mathematics and a memorable analogy.

4.1 The Peltier Effect — Electrons as Heat Carriers

When DC current flows through a junction of two materials with different Seebeck coefficients, heat is absorbed at one junction and released at the other. Discovered by Jean Charles Athanase Peltier in 1834.

$$\mathbf{Q_{Peltier} = \alpha \cdot Tc \cdot I}$$

where α is the total module Seebeck coefficient (V/K), Tc is the cold-side absolute temperature (K), and I is the current (A). For 127-couple ATI modules, αtotal ≈ 0.049–0.052 V/K (at Th = 27 °C, derived from datasheet Vmax/Th,ref).

Analogy — electrons carrying heat backpacks: imagine each electron as a worker carrying a thermal-energy backpack. At the cold junction, workers fill their backpacks with heat from the surrounding lattice; at the hot junction they dump it. More current means more workers per second — and more heat carried — up to a point. The amount each worker can carry depends on the temperature of the loading dock (Tc): warmer dock, bigger backpack. This is why Peltier cooling scales linearly with Tc and gets progressively harder as the cold side gets colder.

Why does α·Tc·I cool rather than heat? Each charge carrier transports a fixed amount of entropy (not just energy) — that is what the Seebeck coefficient measures (units V/K = J/(K·C)). As one coulomb crosses the cold junction, it absorbs entropy α from the cold lattice; thermodynamics requires Q = Tc × α of heat to accompany it. The cold lattice loses that heat. This is reversible entropy transport, fundamentally different from irreversible I^2R Joule heating.

4.2 Joule Heating — The Necessary Evil

Every conductor has electrical resistance, and current through resistance generates heat. Joule heating is unavoidable and works directly against Peltier cooling.

$$\mathbf{Q_{Joule}\ (to\ cold\ side) = \tfrac{1}{2} \cdot R \cdot I^2}$$

The factor of ½ appears because Joule heat is generated uniformly along the length of each pellet — half flows toward the cold side and half toward the hot side. For the ATE1-127-8AS (at 25 °C, 1 kHz AC measurement), $R_{total} \approx 1.52\ \Omega$.

Analogy — workers sweating from effort: the backpack-carrying workers generate body heat from walking. The faster they walk (higher current), the more they sweat. Sweat flows both ways — half back to the cold dock, half to the hot dock. At high current, their own body heat overwhelms the cargo and net cooling collapses. That is why running at I_{max} is wasteful: workers sprinting and sweating barely accomplish anything.

Critical insight: Joule heating scales with I^2 while Peltier cooling scales with I. At low current, linear beats quadratic and Peltier dominates. At high current, the quadratic wins and Joule dominates. This is exactly why there is an optimum current for maximum COP — and it is always well below I_{max}. Section 5.4 makes this trade-off quantitatively visible in the curve library.

4.3 Fourier Conduction — The Leak in the Boat

Heat naturally flows from hot to cold through any thermal conductor. The TEC body itself — Bi_2Te_3 pellets, solder joints, copper traces — provides a path for heat to leak back from the hot side to the cold side, opposing Peltier pumping.

$$\mathbf{Q_{Fourier} = K \cdot \Delta T}$$

where K is the TEC module thermal conductance (W/K) and $\Delta T = Th - Tc$. For the ATE1-127-8AS (computed from the datasheet bridge), $K_{total} \approx 0.65$ W/K.

Analogy — bailing a leaky boat: the Peltier effect is your bucket; you bail water (heat) out of the boat (cold side) and toss it overboard (hot side). Water leaks back through the hole at a rate proportional to the water-level difference (ΔT). At ΔT_{max}, you are bailing exactly as fast as the boat is leaking — net progress is zero. That equilibrium is the physical meaning of ΔT_{max}.

4.4 The Complete Energy Balance

Net cooling at the cold side is Peltier pumping minus the two loss mechanisms:

$$\mathbf{Qc = \alpha \cdot Tc \cdot I - \tfrac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T}$$

This single equation governs ALL TEC performance. Every point on every performance curve, every COP calculation, every design decision traces back to this energy balance.

Heat rejected on the hot side is the cooling power plus total electrical input:

$$\mathbf{Qh = Qc + V \cdot I = Qc + Pin \text{ where } V = \alpha \cdot \Delta T + I \cdot R}$$

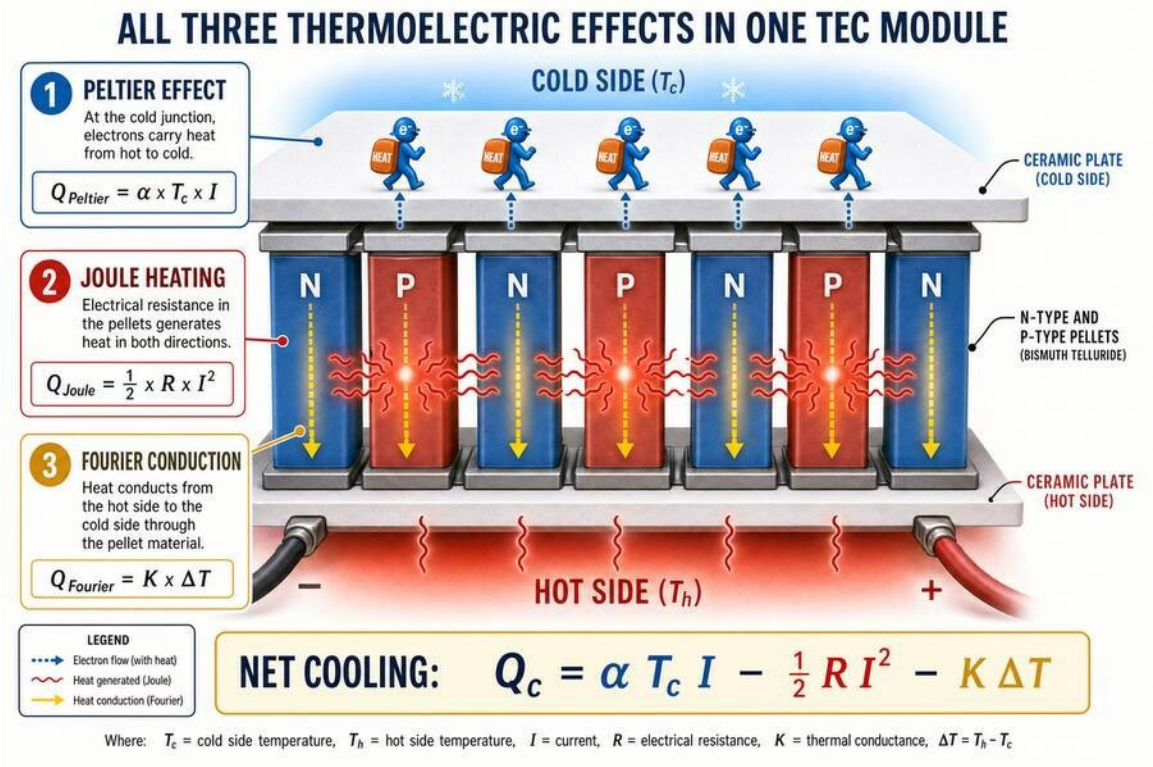

Figure 3: *All three thermoelectric effects in one module. Peltier (α·Tc·I) carries heat from cold to hot via electron transport; Joule (½·R·I²) is bidirectional waste from electrical resistance; Fourier (K·ΔT) leaks heat back from hot to cold by conduction. Net cooling is the Peltier term minus both losses: Qc = α·Tc·I − ½·R·I² − K·ΔT.*

4.5 Why the Optimum Current Is Well Below I_{max}

From the energy balance, the current that maximizes COP (cooling per watt of input power) is:

$I_{opt,COP} = (\alpha \cdot \Delta T) / [R \cdot (\gamma - 1)]$ where $\gamma = \sqrt{(1 + Z \cdot \bar{T})}$ and $\bar{T} = (Th + Tc)/2$

For typical conditions (ΔT = 20–30 °C, Th = 30–50 °C, Z ≈ 2.4 × 10^{-3} K^{-1}), this works out to I/I_{max} ≈ 0.20–0.35 — what we call the "Goldilocks zone." Operating here: COP is maximized (typically 1.5–4), Joule heating is minimized (I^2 is small), the heat sink handles less total heat, module lifetime is maximized (less thermal stress), and temperature stability is best (less self-heating feedback).

Note on COP Values: The tabulated and plotted COP values represent ideal module behavior with perfect thermal interfaces. In real systems, COP is typically 15–25% lower due to temperature-dependent material properties, TIM resistance, and heat-sink thermal resistance. At ΔT/ΔTmax > 0.5, expect COP 20–40% lower than the ideal curves shown.

Design Rule: When using the COP curves in Figures 7 and 8, derate by 15–25% for first-pass system sizing. Use the exact energy balance with measured α, R, K values (available from ATI on request) for final validation.

The Goldilocks zone is the single most important operating recommendation in this paper. Section 5.4 makes it quantitative through the COP-versus-I/I_{max} curve, where you can see exactly how COP peaks in the 0.20–0.35 band and collapses on either side.

DESIGN RULE — THE GOLDILOCKS ZONE: For maximum lifetime and efficiency, operate your TEC at I/Imax = 0.20 to 0.35. This current range delivers 80–95% of the maximum achievable COP while keeping Joule heating manageable and thermal-cycling stress low. Oversizing the module (Qmax ≥ 4× Qc) is what makes this zone accessible.

Quick answer: *A TEC's net cooling is $Q_c = \alpha \cdot T_c \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$ — Peltier minus Joule minus Fourier; the COP-optimum current sits at I/I_{max} = 0.20–0.35 because Peltier scales with I while Joule scales with I^2.*

The following cartoon distills the energy-balance competition into a single memorable image. Think of the TEC as a hill: the Peltier effect is a worker hauling ice balls (heat packets) uphill from the cold plate to the hot plate. His effort is proportional to current ($\alpha \cdot T_c \cdot I$). But effort has a cost: Joule self-heating ($\frac{1}{2} R \cdot I^2$) produces fire balls — sweat from the exertion — that warm both sides. Simultaneously, Fourier conduction ($K \cdot \Delta T$) sends ice balls rolling back downhill, undoing the Peltier work. The three panels below show why there is a sweet spot: too little current and Peltier barely pumps; too much current and Joule overwhelms everything; at $I = I_{max}$ the worker barely wins against maximum back-

conduction, achieving ΔT_{max}. For best COP, operate well below this limit — in the Goldilocks zone ($I/I_{max} \approx 0.2–0.35$) where Peltier dominates and Joule is still small.

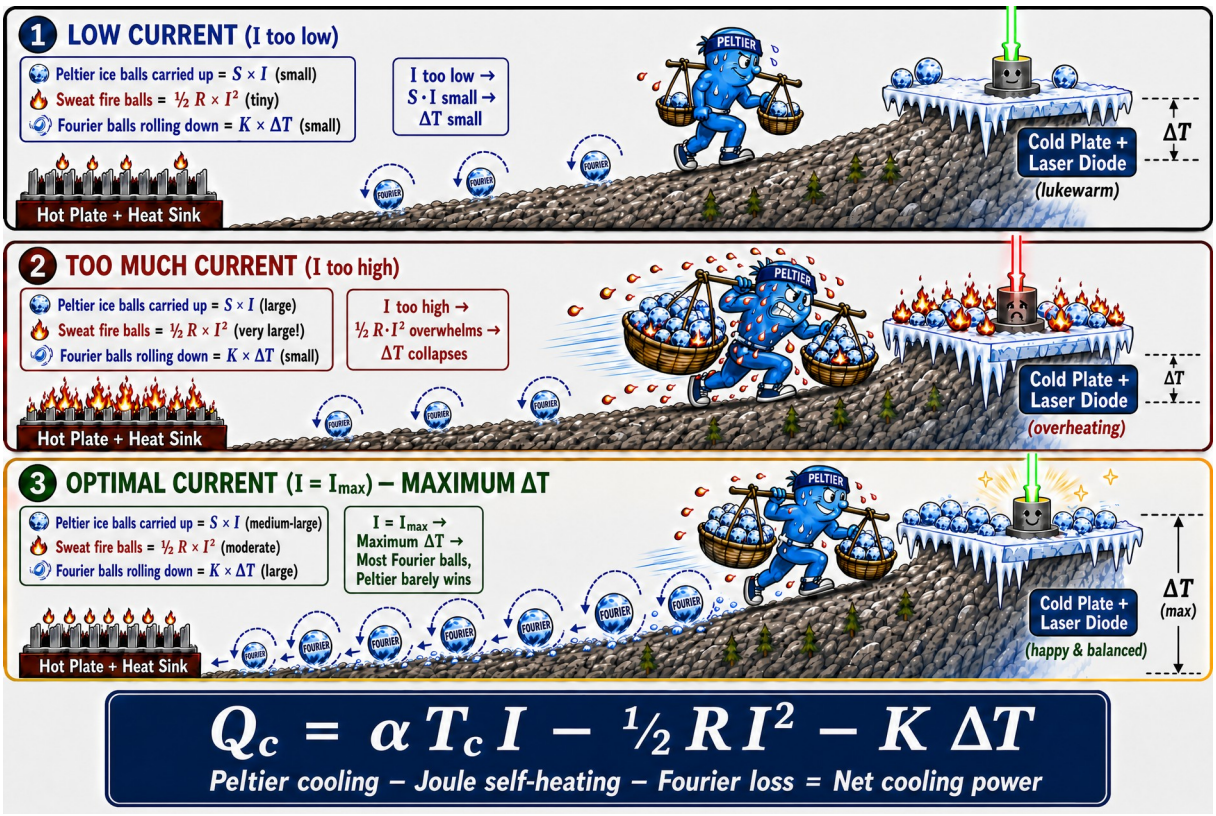

Figure 4: The Peltier-vs-losses tug of war — why the COP-optimum current is below Imax. The blue Peltier character carries ice balls (cooling power α·Tc·I) uphill from the cold plate to the hot plate. His sweat drops are Joule fire balls (½R·I²) that heat both sides. Meanwhile, Fourier ice balls (K·ΔT) roll back downhill by thermal conduction. Panel 1 (top): at low current, Peltier barely carries any ice — ΔT is small. Panel 2 (middle): at excessive current, Joule sweat overwhelms Peltier — ΔT collapses. Panel 3 (bottom, gold border): near the maximum-ΔT condition. At Qc = 0, I = Imax produces ΔTmax, but this is not the COP-optimum operating point. For best COP, operate well below this limit, typically at I/Imax ≈ 0.20–0.35. At this limit, Peltier pumping only barely exceeds maximum Fourier back-flow, achieving the largest possible temperature difference ΔT_{max}. The master equation Qc = α·Tc·I − ½·R·I² − K·ΔT governs all three regimes. *Note: In this figure, S = α = module-level Seebeck coefficient (engineering alias). The master equation uses α throughout the paper.*

5. TEC Performance, Specifications, and Thermal Network — The Complete Technical Reference

Section 4 established the physics. This chapter turns that physics into engineering you can use. The path is deliberately step-by-step: we start from the four numbers printed on every TEC datasheet, extract the underlying material parameters, define the coefficient of performance and the Goldilocks zone, then unfold the complete normalized performance-curve library that lets you predict any operating point. The curves all assume the datasheet's reference hot-side temperature, so we follow with the advanced theory of how ΔT_{max} shifts when Th changes. The chapter closes by stepping out from the TEC module to the system — designing the hot-side thermal network so the heat sink actually delivers the Th the curves assume.

Read this chapter once start-to-finish and you will own everything needed to specify, predict, and surround any TEC module with a working thermal system. Skim it later, by subsection, as a working reference whenever you need a number.

5.1 Reading the TEC Datasheet — Four Numbers That Determine Everything

Every TEC module datasheet specifies the same four values at a reference hot-side temperature (typically Th = 27 °C). They are the universal currency of TEC engineering — everything that follows in this chapter, and indeed in this entire paper, is computed from these four numbers plus the energy balance from Section 4. Download the ATE1-127 datasheet to follow along.

Parameter	Meaning	Symbol	ATE1-127-8AS
Maximum cooling capacity	Heat pumped when ΔT = 0 (cold side = hot side)	Q_{max}	68.9 W
Maximum temperature difference	ΔT at zero heat load (Qc = 0)	ΔT_{max}	66 °C
Maximum current	Current that produces ΔT_{max} (at Qc = 0)	I_{max}	8.0 A
Maximum voltage	Voltage across module at I_{max}	V_{max}	15.4 V

Parameter	Meaning	Symbol	ATE1-127-8AS
	and ΔT_{max}		

Two practical notes. First, Q_{max} is a theoretical upper bound — it occurs only when there is no temperature difference (Tc = Th), a condition that never holds in a working system because the cold side is colder than the hot side by definition. Real cooling capacity is always lower than Q_{max}. Second, ΔT_{max} assumes zero useful cooling load; any heat the cold side must actually remove cuts into ΔT_{max} linearly. The whole curve library in 5.4 is a quantitative map of how Q_{max} shrinks with ΔT and how ΔT_{max} shrinks with load.

These four numbers describe what the TEC module can do; the next step is to extract what the TEC module is made of — its underlying α, R, K, and Z. With those, every performance curve in the rest of this chapter follows from a single equation.

5.2 Deriving the Physics from the Datasheet

The four datasheet specifications correspond uniquely to four physical parameters: the Seebeck coefficient α, the electrical resistance R, the thermal conductance K, and the figure of merit $Z = \alpha^2/(R \cdot K)$. The closed-form bridge between datasheet and physics is:

$$\alpha = V_{max} / Th \quad R = (Th - \Delta T_{max}) \cdot V_{max} / (Th \cdot I_{max}) \quad K = (Th - \Delta T_{max}) \cdot V_{max} \cdot I_{max} / (2 \cdot Th \cdot \Delta T_{max}) \quad Z = \alpha^2 / (R \cdot K)$$

Use Th in Kelvin (so Th = 27 °C means 300 K). Apply to the TEC module at Th = 300 K, ΔT_{max} = 66 °C, I_{max} = 8 A, V_{max} = 15.4 V: Note: The slight (5–10%) discrepancy between bridge-derived and 1-kHz measured values arises from temperature-dependent transport coefficients; we use bridge values throughout the worked examples for didactic consistency. All subsequent calculations use $Z = 2.41 \times 10^{-3}$ K^{-1} (derived from the datasheet reference: $2 \cdot 66/234^2 = 2.41 \times 10^{-3}$).

Let Tc,ref ≡ Th,ref − ΔTmax (the datasheet cold-side reference temperature). For the ATE1-127-8AS: Tc,ref = 300 − 66 = 234 K.

Parameter	Meaning	Computation	Value
α	Seebeck coefficient — voltage per kelvin	15.4 / 300	0.0513 V/K (≈ 0.049 measured)
R	Electrical resistance of the TEC module	(300 − 66) · 15.4 / (300 · 8)	1.50 Ω (≈ 1.52 measured)
K	Thermal conductance — heat leak at I=0	234 · 15.4 · 8 / (2 · 300 · 66)	0.728 W/K (≈ 0.652 measured)

Parameter	Meaning	Computation	Value
Z	Figure of merit — material quality factor	α^2 / (R·K)	2.41×10^{-3} K^{-1}

The simplified datasheet-bridge formulas give slightly different values from the measured ones (in parentheses) because real Bi_2Te_3 has temperature-dependent parameters and the bridge formulas assume constant α, R, K. The discrepancy is small enough (5–10%) that the bridge values are entirely adequate for first-pass engineering. For high-accuracy work, ATI provides measured α, R, K on request.

With these four numbers — α, R, K, Z — you can now predict every quantity the TEC does at every operating point through the energy balance $Q_c = \alpha \cdot T_c \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$ and the voltage law $V = \alpha \cdot \Delta T + I \cdot R$. The next subsections take that prediction in three useful directions: efficiency (COP), the full curve library, and the dependence of ΔT_{max} on Th.

$$V = \alpha \cdot \Delta T + I \cdot R \quad \text{(TEC Terminal Voltage Law)}$$

This is the Seebeck back-EMF (α·ΔT) plus the Ohmic drop (I·R). It determines the voltage your controller must supply at any operating point.

Note: The ½ factor in Joule heating is the standard constant-property approximation, which assumes that I^2R self-heating is split equally between the cold and hot faces. Real devices show slight asymmetry due to temperature dependence of resistivity and the Thomson effect, but this model introduces <5% error and is the industry-standard engineering approach used by all major TEC manufacturers.

Before we plot the curves, one efficiency metric deserves its own discussion — because it dictates where on those curves you actually want to operate.

5.3 Coefficient of Performance and the Goldilocks Zone

[Canonical Sizing Rule] The Qmax-to-Qc oversizing rule depends on your design target. A single multiplier does not fit every application. Use the following canonical rule: Minimum size (footprint-constrained): Qmax/Qc = 1.5–2×, I/Imax ≈ 0.9–1.0, COP 0.3–0.8. Balanced (general precision work): Qmax/Qc = 4–6×, I/Imax ≈ 0.20–0.35 (Goldilocks zone), COP 1.3–2.5. Maximum efficiency (battery, dense enclosure): Qmax/Qc = 5–8×, I/Imax ≈ 0.15–0.25, COP 2.5–4.0. Maximum ΔT (deep cooling): Qmax/Qc = 10×+, I/Imax ≈ 0.9–1.0, COP 0.1–0.5. Most precision applications belong in the Balanced row. Quick Answers and selection tables elsewhere in this paper use that target unless explicitly noted. §6.5 (Three Ways to Design a TEC System) walks through all four targets with closed-form formulas.

Canonical sizing rule (master reference): The Qmax-to-Qc ratio depends on the design target. Use 1.5–2× for minimum-size designs (highest current, lowest COP), 4–6× for balanced precision designs (ATI default recommendation), 6–8× for maximum COP/lifetime, and 8–10×+ or multi-stage for maximum-ΔT. The 4–6× range keeps the operating current in the Goldilocks zone (I/Imax ≈ 0.20–0.35) and minimizes hot-side heat-sink burden.

Warning: Driving a TEC at Imax is appropriate only for maximum-ΔT characterization or short-duty extreme cooling. It is not the recommended operating point for precision systems or long lifetime. Continuous operation near Imax produces low COP, large waste heat, high solder/interconnect stress, and requires an aggressively sized heat sink. For normal precision control, use the COP-optimized range I/Imax ≈ 0.20–0.35.

The coefficient of performance (COP) is the ratio of useful cooling to electrical input power:

$$\mathbf{COP = Qc / Pin = Qc / (V \cdot I)}$$

COP varies dramatically with operating point — and the variation is the difference between a good design and a power-hungry, heat-sink-saturating one. The following table shows representative COP values for the TEC module at Th = 27 °C:

Operating point	Typical COP	Practical meaning
I = Imax, ΔT = ΔT_{max}	~0	All power goes to maintaining ΔT; no useful cooling
I = Imax, ΔT = 0	~0.76	Maximum cooling but poor efficiency
I = 0.5·Imax, ΔT = 30 °C	0.6–0.9	Workable but expensive in wall power
I = 0.3·Imax, ΔT = 20 °C	1.0–1.5	Good cooling with reasonable efficiency
I = 0.2·Imax, ΔT = 10 °C	2.0–3.0	Excellent efficiency, moderate cooling
I = 0.15·Imax, ΔT = 5	3.0–4.0	Maximum efficiency,

Operating point	Typical COP	Practical meaning
°C		minimum waste heat

The Goldilocks zone is I/I_{max} = 0.20–0.35 — the band where COP peaks across the full ΔT range, Joule heating is small, the heat sink stays cool, and module lifetime is maximized. Drive harder and Joule heat dominates; drive softer and Peltier pumping is wasted.

The reason this band exists, mathematically: Peltier cooling scales linearly with I (α·Tc·I), while Joule loss scales quadratically (½·R·I^2). At low current the linear term dominates and COP improves with current; at high current the quadratic catches up and COP collapses. The crossover sits near I/I_{max} = 0.25 for typical Bi_2Te_3 at room temperature, with mild dependence on ΔT. Subsection 5.4 plots this directly as Curve 4 — and you can read the optimum current ratio off the figure.

One short engineering rule captures the design implication of the Goldilocks zone:

Size your TEC so that Q_{max} is 2× to 4× your cooling load Qc. This forces the operating current into the Goldilocks zone automatically.

Single numbers and single rules only get you so far. The full landscape of TEC behavior — how cooling, voltage, power, heat rejection, and efficiency all move together — is best seen as a family of normalized curves. That library is next.

5.3.1 Optimizing COP — The Exact Solution

The following table defines all symbols used in this section. Readers may refer back to this table at any point during the derivation.

Symbol	Name	Definition / Meaning	Units
Qc	Cooling load	Heat to be removed from the cold object	W
Tc	Cold-side temperature	Temperature of the object being cooled (absolute)	K
Th	Hot-side temperature	TEC hot face temperature = Tc + ΔT	K
Tamb	Ambient temperature	Maximum ambient air	K

Symbol	Name	Definition / Meaning	Units
		temperature	
ΔT = Th - Tc	Temperature lift	Actual temperature difference across the TEC	K
ΔT_{max}	Max temperature diff.	Module datasheet maximum ΔT (at Imax, Qc=0)	K
I_{max}	Maximum current	Module datasheet rated maximum current	A
V_{max}	Maximum voltage	Module datasheet rated maximum voltage	V
Q_{max}	Maximum cooling	Module datasheet maximum Qc (at DT=0, I_{max})	W
Th,ref	Reference hot temp.	Hot-side temp during datasheet measurement (typ. 300 K)	K
Tc,ref = Th,ref - ΔTmax	Reference cold temp.	Cold-side temp at ΔT_{max} conditions	K
$Z = 2\Delta Tmax/(Th,ref - \Delta Tmax)^2$	Figure of merit	Thermoelectric material quality factor	1/K
$\theta = \Delta T/\Delta T_{max}$	Normalized lift	Fraction of module capacity used for temperature lift	—
$\gamma = \sqrt{(1+Z\cdot\bar{T})}$	Ioffe parameter	Thermoelectric performance parameter (typ. 1.30-1.34)	—
$\bar{T} = (Th+Tc)/2$	Mean temperature	Average absolute temperature across the TEC	K
$i_{opt} = Iopt/I_{max}$	Normalized opt. current	Optimum current as fraction of I_{max} for max	—

Symbol	Name	Definition / Meaning	Units
		COP	
v_{opt} = **Vopt/V_{max}**	Normalized opt. voltage	Optimum voltage as fraction of V_{max} for max COP	—
qopt = **Qc,avail/Qmax**	Normalized cooling	Fraction of Q_{max} available at optimum current	—
COP_{max}	Maximum COP	Best possible coefficient of performance at given ΔT	—
Qmax,min	Min. module rating	Smallest module Q_{max} that can deliver Qc at COP_{max}	W
Rhs,max	Max hot-side resistance	Largest allowable thermal resistance, hot side to ambient	K/W

Starting from the energy balance $Q_c = \alpha \cdot T_c \cdot I - \tfrac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$ and setting $d(COP)/dI = 0$ (Ioffe, 1957; Goldsmid, 1954), the optimum current for maximum COP is:

where α is the Seebeck coefficient, R is electrical resistance, $\gamma = \sqrt{(1+Z \cdot \bar{T})}$ is the Ioffe parameter, $\bar{T}$ is the mean absolute temperature, and Z is the figure of merit. Physically, $\gamma - 1$ measures the irreversibility budget of the module: as $\gamma \to 1$ ($Z \cdot \bar{T} \to 0$), COP→0; as $\gamma \to \infty$ (ideal thermoelectric), COP approaches Carnot.

$$I_{opt} = \alpha \cdot \Delta T / [R \cdot (\gamma - 1)]$$ (Ioffe, 1957; Goldsmid, 1954)

where $\gamma = \sqrt{(1 + Z \cdot \bar{T})}$ is the Ioffe parameter, $\bar{T} = (T_h + T_c)/2$ is the mean absolute temperature, and $Z = 2 \cdot \Delta T_{max} / (T_{h,ref} - \Delta T_{max})^2$ is the thermoelectric figure of merit extracted from the datasheet. For typical Bi_2Te_3 near room temperature, $Z \cdot \bar{T} \approx 0.7–0.8$, giving $\gamma \approx 1.30–1.34$.

In normalized form, dividing by $I_{max} = \alpha \cdot T_{c,ref} / R$:

where $\theta = \Delta T/\Delta T_{max}$ is the normalized temperature lift, iopt is the optimum current fraction, and $T_{c,ref}$ is the cold-side reference temperature.

$$i_{opt} = I_{opt} / I_{max} = \theta \cdot \Delta T_{max} / [T_{c,ref} \cdot (\gamma - 1)] \approx 0.89 \cdot \theta$$

The corresponding optimum voltage (dividing by $V_{max} = \alpha \cdot T_{h,ref}$):

where vopt is the optimum voltage fraction and Th,ref is the hot-side reference temperature.

$$vopt = Vopt / Vmax = \theta \cdot \Delta Tmax \cdot \gamma / [(\gamma - 1) \cdot Th,ref] \approx 0.91 \cdot \theta$$

The maximum COP at this optimum current:

where Tc is the absolute cold-side temperature, Th is the absolute hot-side temperature, and ΔT = Th - Tc.

$$COP_{max} = (Tc/\Delta T) \cdot (\gamma - Th/Tc) / (\gamma + 1)$$

The first factor Tc/ΔT is the Carnot COP — the theoretical maximum for any heat pump operating between Tc and Th. The second factor $(\gamma - Th/Tc)/(\gamma + 1)$ is the TEC's thermodynamic efficiency relative to Carnot, depending only on Z and the operating temperatures. For typical Bi_2Te_3 at room temperature ($Z\cdot\bar{T} \approx 0.7$), this efficiency factor is 0.10–0.25.

Physical insight: all four design quantities (iopt, vopt, Pin, COP) scale with a single parameter θ = ΔT/ΔTmax. Halving θ roughly cuts input power by 4× and can nearly double COP, but it requires a significantly larger Qmax rating, often approaching 2× depending on the operating range. This is the fundamental cost-vs-efficiency trade-off in TEC system design.

5.3.2 Normalized Form and Quick-Estimate Rules

The simple approximations $i_{opt} \approx 0.89 \cdot \theta$ and $v_{opt} \approx 0.91 \cdot \theta$ are accurate to within ±5% across the practical design range ($0.1 < \theta < 0.5$). They arise because γ varies slowly with temperature for Bi_2Te_3 ($\gamma \approx 1.30$–1.34 across −20 to +50 °C cold-side range).

where θ = ΔT/ΔTmax (normalized temperature lift), γ = √(1 + Z·T̄) (Ioffe parameter), iopt = Iopt/Imax (normalized optimum current), vopt = Vopt/Vmax (normalized optimum voltage), and Rhs,max = maximum allowable hot-side thermal resistance.

All four design quantities scale with θ:

Quantity	Scaling with θ	Implication
$\mathbf{i_{opt}}$	∝ θ	Lower θ → lower current → longer lifetime
$\mathbf{v_{opt}}$	∝ θ	Lower θ → lower voltage → simpler driver
PTEC	∝ θ^2	Halving θ cuts input power by 4×

Quantity	Scaling with θ	Implication
COP	∝ 1/θ	Halving θ doubles efficiency
Qmax,min	∝ 1/θ	Lower θ → larger (more expensive) module

Complete Design Algorithm:

1. Extract $Z = 2 \cdot \Delta T_{max} / (T_{h,ref} - \Delta T_{max})^2$ from the datasheet

2. Choose target θ (start with θ = 0.3 for balanced design)

3. Compute: $T_h = T_c + \theta \cdot \Delta T_{max}$, $\bar{T} = (T_h + T_c)/2$, $\gamma = \sqrt{(1 + Z \cdot \bar{T})}$

4. Compute: $i_{opt} \approx 0.89 \cdot \theta$, $v_{opt} \approx 0.91 \cdot \theta$

5. Compute required module: $Q_{max,min} = Q_c / (0.54 \cdot \theta + 0.034)$

6. Compute heat sink: $R_{hs,max} = (T_h - T_{amb}) / [Q_c \cdot (1 + 1/COP_{max})]$

7. Verify feasibility: $Q_{max,min} \leq$ module Q_{max}? Rhs achievable? $i_{opt} < 0.5$?

8. If not feasible: increase θ (accept lower COP) or choose larger module

Rule of thumb: For COP > 1, choose $Q_{max} \geq 5 \times Q_c$ and ensure θ < 0.35. The Goldilocks zone (i_{opt} = 0.20–0.35, θ = 0.22–0.39) represents the sweet spot where COP is good (1.3–2.6), the module is reasonably sized (4–6× Qc), and lifetime exceeds 200,000 hours (steady-state, $T_h \leq 50$ °C, sealed, proper clamping).

5.3.3 Module Selection for Maximum COP

At the COP-optimum current, the module delivers a cooling power $Q_{c,avail}$ that is less than its rated Q_{max}. The ratio $q_{opt} = Q_{c,avail} / Q_{max}$ determines how much "oversizing" is needed:

$$Q_{max,min} = Q_c / q_{opt}(\theta)$$

where q_{opt} is the normalized cooling at the COP-optimum current:

where $q_{opt} = Q_{c,avail}/Q_{max}$ is the fraction of maximum cooling capacity available at the optimum efficiency point.

$$q_{opt} = (2/T_{c,ref}^2) \cdot [T_c \cdot \Delta T/(\gamma - 1) - \Delta T^2/(2(\gamma - 1)^2) - \Delta T/Z]$$

Practical approximation (±10% for 0.1 < θ < 0.5):

where Qmax,min is the minimum required module datasheet rating, Qc is your actual cooling load, and θ is the normalized lift.

$$q_{opt} \approx 0.54 \cdot \theta + 0.034$$

$$Qmax,min \approx Qc / (0.54 \cdot \theta + 0.034)$$

Module Selection Table (Qmax,min / Qc vs. θ), where θ = ΔT/ΔTmax is the normalized temperature lift:

θ	Qmax,min / Qc	Interpretation
0.10	12.5×	Very oversized — extremely high COP
0.15	8.7×	Large module, COP ≈ 3.6
0.20	6.8×	Good balance of size and efficiency
0.25	5.7×	Moderate oversizing, COP ≈ 2.0
0.30	5.0×	Standard design point, COP ≈ 1.6
0.35	4.5×	Compact design, COP ≈ 1.3
0.40	4.1×	Minimum practical oversizing, COP ≈ 1.1
0.50	3.7×	Near minimum, COP < 1

The maximum allowable hot-side thermal resistance:

where Rhs,max is the maximum allowable thermal resistance from the TEC hot side to ambient, and Tamb is the maximum ambient temperature.

$$Rhs,max = (\theta \cdot \Delta Tmax + Tc - Tamb) / [Qc \cdot (1 + 1/COPmax)]$$

If Rhs,max < 0, the design is infeasible — the ambient is too hot for the chosen θ. Either increase θ (accept lower COP) or improve the heat sink.

For the ATE1-127 series, the following modules cover most practical applications:

• ATE1-127-5AS (Q_{max} = 43 W): laser diodes, small sensors, fiber-optic components

- ATE1-127-8AS (Q_{max} = 68.9 W): CCD/CMOS imagers, analytical instruments
- ATE1-127-12AS (Q_{max} = 100 W): large detectors, multi-chip assemblies
- ATE1-127-15AS (Q_{max} = 120 W): AI accelerator hotspots, high-power amplifiers

5.3.4 The Negative-ΔT Regime — Active Heat Spreading

In this regime, the convention of Section 4 is reversed: the 'cold side' in our equations is physically warmer than the 'hot side,' so $\Delta T = Th - Tc < 0$ using the standard sign convention. The TEC assists natural heat flow rather than opposing it, which is why COP can exceed 10 in the negative-ΔT active heat-spreading regime (not sub-ambient cooling).

When the TEC cold side is warmer than the hot side ($\Delta T < 0$), the Peltier effect supplements natural heat conduction rather than fighting it. In this regime:

- COP can exceed 10 (even 15–20 for very small $|\Delta T|$)
- The required current is very low ($i < 0.15$)
- Input power is minimal — a few watts can move tens of watts of heat

This "active heat spreading" mode is increasingly important in AI accelerator and high-power electronics cooling, where the goal is not to cool below ambient but to reduce local hotspot temperatures. A TEC operating in this regime acts as a thermal "equalizer," actively pumping heat from a concentrated hotspot to a larger heat-spreading surface. See Example C (Section 9.3) for a complete worked design.

5.3.5 Numerical Verification

Test case: Qc = 20 W, Tc = 20 °C (293 K), Tamb = 30 °C, Rhs = 0.20 °C/W

Module: ATE1-127-8AS (ΔT_{max} = 66 K, I_{max} = 8 A, V_{max} = 15.4 V, Q_{max} = 68.9 W)

Parameter	Exact	Approximation	Error	**Error**
θ (normalized lift)	0.300	—	—	—
γ (Ioffe parameter)	1.316	—	—	—
iopt	0.268	0.89 × 0.300 = 0.267	−0.5%	+0.9%
vopt	0.265	0.91 × 0.300 = 0.273	+3.0%	+0.1%
COPmax	1.585	—	—	—

Parameter	Exact	Approximation	Error	**Error**
Qmax,min	102 W	20 / (0.54·0.300 + 0.034) = 102 W	0%	+2%
Rhs,max	Max. hot-side thermal resistance to ambient	0.302 °C/W	—	—

The simple approximations (iopt ≈ 0.89·θ, vopt ≈ 0.91·θ, Qmax,min ≈ Qc/(0.54·θ + 0.034)) are accurate to within ±5% across the practical design range (0.1 ≤ θ ≤ 0.6). Engineers can use these for rapid first-pass sizing, then refine with the exact formulas. Verification at θ = 0.300: iopt,exact = 0.268 vs. 0.89×0.300 = 0.267 (−0.5%); vopt,exact = 0.265 vs. 0.91×0.300 = 0.273 (+3.0%); Qmax,min,exact = 102 W vs. 20/(0.54×0.300+0.034) = 102 W (0%).

5.4 The Normalized Performance Curve Library

The seven charts that follow are the engineering reference for the ATE1-127 series. Each is normalized to the datasheet basic specs (Qmax, Vmax, Imax, ΔT_{max}) so it applies directly to any module in the ATE1-127 series — and to any 127-couple Bi_2Te_3 TEC with comparable figure of merit. Only the last chart (5.5, ΔT_{max} vs Th) uses absolute Celsius, because the question it answers is intrinsically about real hot-side temperatures. These curves apply to all modules in the ATE1-127 series — simply multiply by the datasheet Qmax, Imax, or V_{max} to obtain absolute values.

Assumptions for all normalized curves: single-stage 127-couple Bi_2Te_3 module; constant-property model; Th,ref = 27 °C (300 K) unless stated otherwise. Real modules may deviate ±5–10% due to temperature-dependent material properties.

All curves were generated from the Section 4 energy balance $Qc = \alpha \cdot Tc \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$ using the reference module (ATE1-127-8AS) module parameters at Th = 27 °C. To apply them to any other variant in the ATE1-127 series, multiply the y-axis value by that variant's datasheet Q_{max} (or Vmax, Imax, etc.) to recover absolute watts, volts, or amps.

Curve 1 — Cooling Capacity Qc/Q_{max} vs. $\Delta T/\Delta T_{max}$

This is the single most useful chart in TEC design. Pick your normalized operating point ($\Delta T/\Delta T_{max}$ on the x-axis, Qc/Q_{max} on the y-axis) and read off the required current ratio. Cooling capacity drops approximately linearly with ΔT for any fixed current; the slope is set by the thermal conductance K, and the four currents fan out into four parallel lines. The shaded band marks the typical design target Qc/Q_{max} = 0.20–0.40.

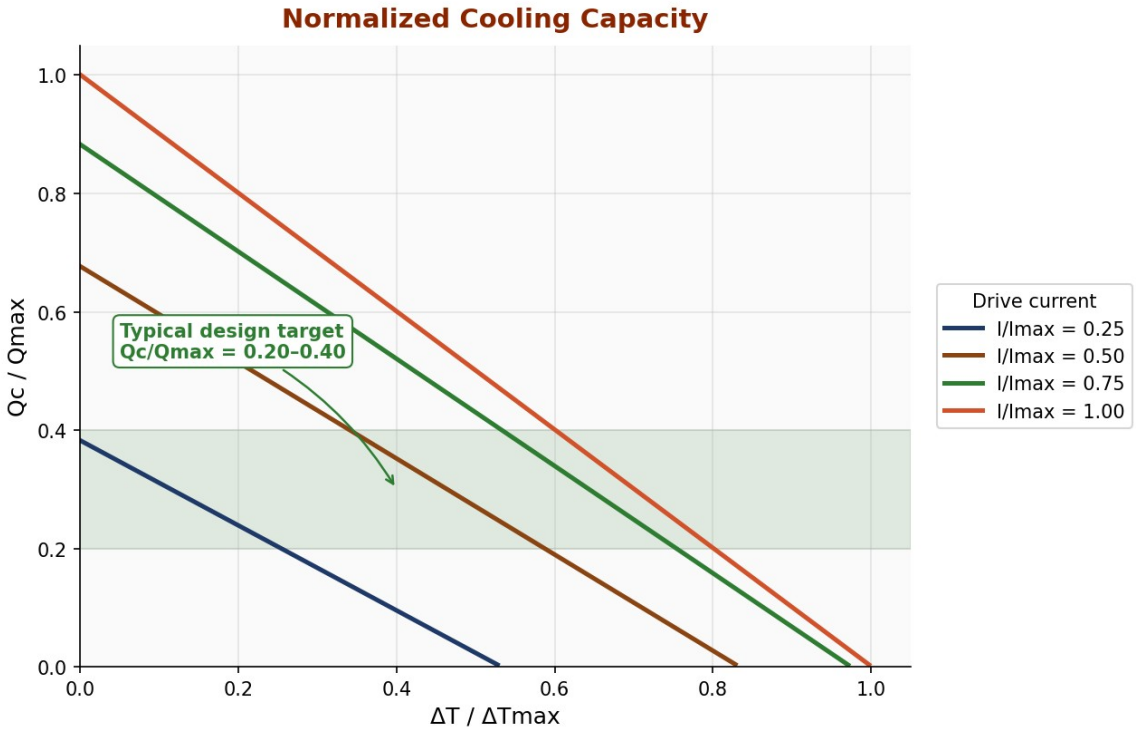

Figure 5: *Normalized cooling capacity Qc/Q_{max} vs. normalized temperature difference $\Delta T/\Delta T_{max}$ at four drive currents. To use: enter at your required $\Delta T/\Delta T_{max}$ on the x-axis, project up to your candidate current ratio, and read Qc/Q_{max} — then multiply by the TEC module's datasheet Q_{max} to get absolute cooling watts.*

Curve 2 — Terminal Voltage V/V_{max} vs. $\Delta T/\Delta T_{max}$

Predicts the TEC module voltage required at any operating point so you can size the controller's output rail. V/V_{max} climbs with both current and ΔT because $V = \alpha \cdot \Delta T + I \cdot R$ — the Seebeck back-EMF ($\alpha \cdot \Delta T$) and the resistive drop ($I \cdot R$) add. Many engineers size controllers by current alone; this chart prevents the common follow-on mistake of running out of voltage headroom at large ΔT.

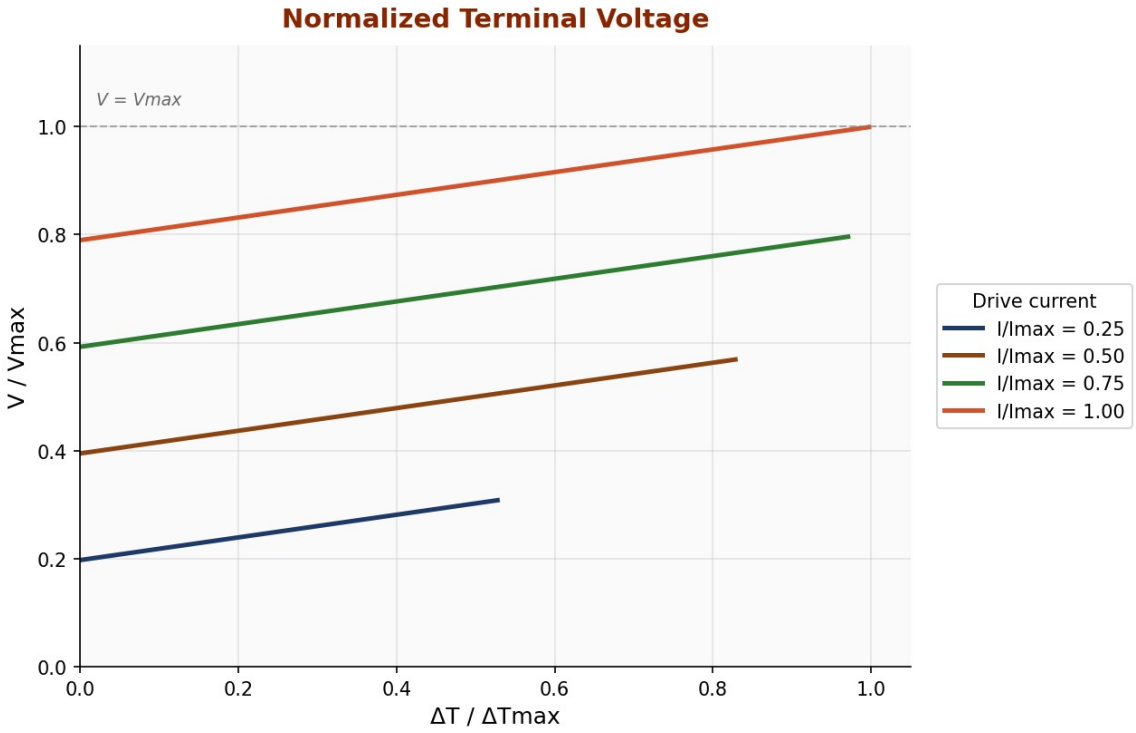

Figure 6: Normalized terminal voltage V/V_{max} vs. $\Delta T/\Delta T_{max}$ at four drive currents. Multiply V/V_{max} by the module's datasheet V_{max} (15.4 V across the ATE1-127 series) to recover the absolute terminal voltage required at the operating point.

Curve 3 — Efficiency COP vs. $\Delta T/\Delta T_{max}$

Coefficient of Performance vs. normalized temperature difference, plotted at six current ratios. At small ΔT and low I/Imax, COP climbs above 3 — this is where TECs are most efficient. As ΔT approaches ΔT_{max}, COP collapses to zero for any current; the TEC module spends all its electrical input fighting the Fourier back-conduction K·ΔT and has nothing left for useful cooling.

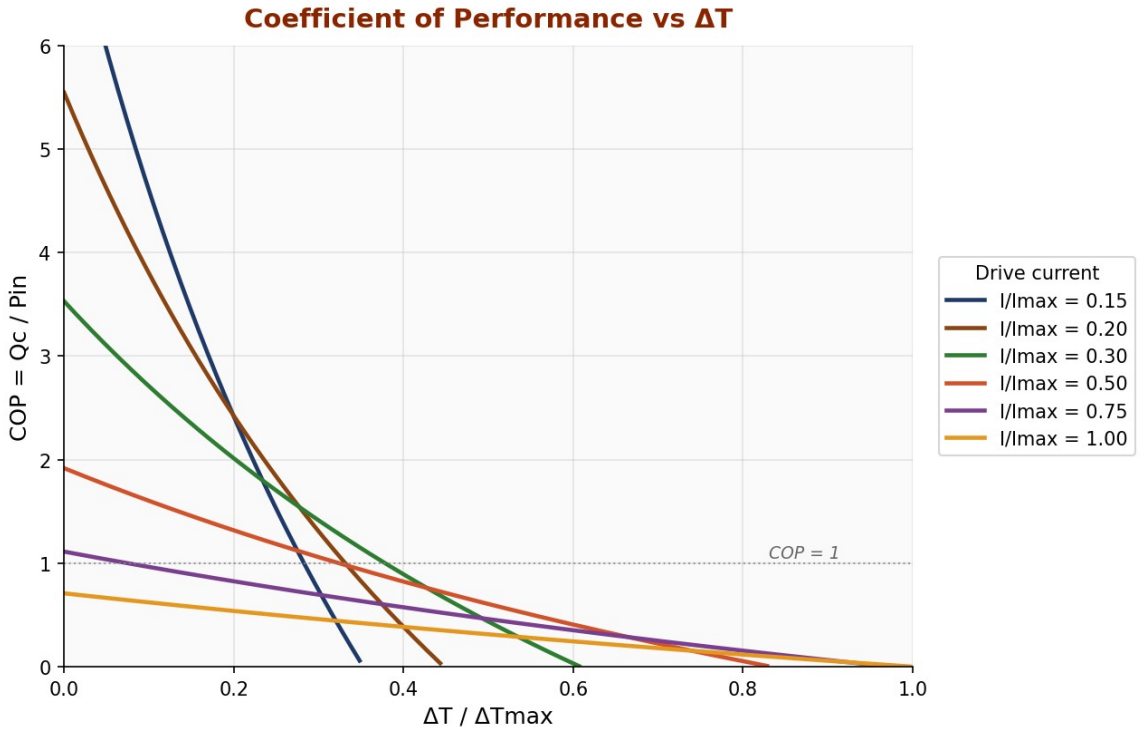

Figure 7: *Coefficient of Performance vs. $\Delta T/\Delta T_{max}$. Each curve represents a fixed drive current. The dotted line at COP = 1 marks the break-even point where electrical input equals cooling output. Below it, the TEC consumes more wall power than it removes as heat.*

Curve 4 — The Goldilocks Zone: COP vs. I/I_{max}

The chart that justifies the central operating recommendation of this paper. At every $\Delta T/\Delta T_{max}$ loading there is an optimum current ratio that maximizes COP. Track the peaks of the six curves and they cluster in the band I/I_{max} = 0.20–0.35 — the Goldilocks zone. Drive harder and Joule heating collapses efficiency; drive softer and Peltier pumping is left on the table.

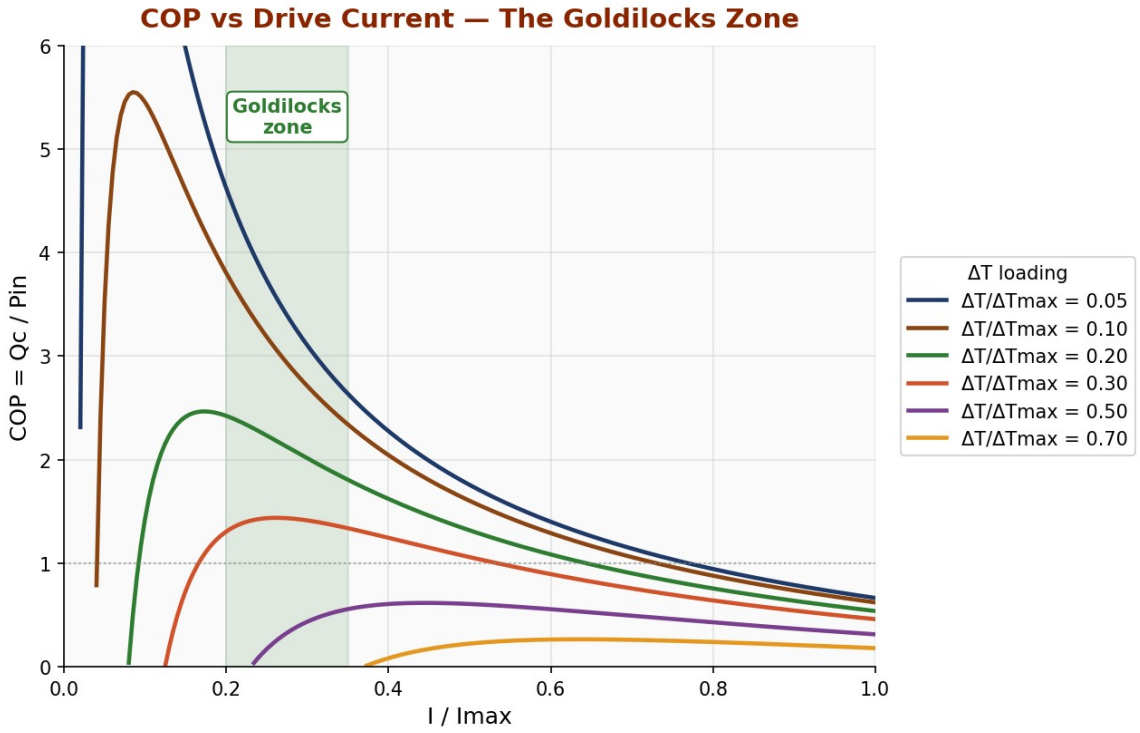

Figure 8: *COP vs. drive-current ratio I/I_{max} for several ΔT loadings. The green band highlights I/I_{max} = 0.20–0.35, the recommended operating range. Notice how the peaks of all six curves fall inside the band, regardless of ΔT — this is why the Goldilocks rule is a useful first-pass design rule across the* ATE1-127 series.

Curve 5 — Heat Rejection Qh/Q_{max} vs. $\Delta T/\Delta T_{max}$

This is the sizing curve for the hot side. The heat sink must reject Qh = Qc + Pin, which is always larger than Qc and can exceed Q_{max} at high I/I_{max}. Read Qh/Q_{max} at your operating point and multiply by the datasheet Q_{max} to get absolute watts of waste heat — that number, not Qc, sets the heat-sink thermal resistance in 5.6.

Sign convention for bidirectional (heating) operation: When the TEC is driven in reverse (current reversed), the roles of hot and cold faces swap. In heating mode, the device being heated receives Qheat = Qc + Pin — both the Peltier-pumped heat AND the Joule heat arrive at the target. The heating COP is COPheating = COPcooling + 1, which is always > 1. All equations in this paper assume cooling mode (positive current = cold side absorbs Qc); reverse polarity for heating.

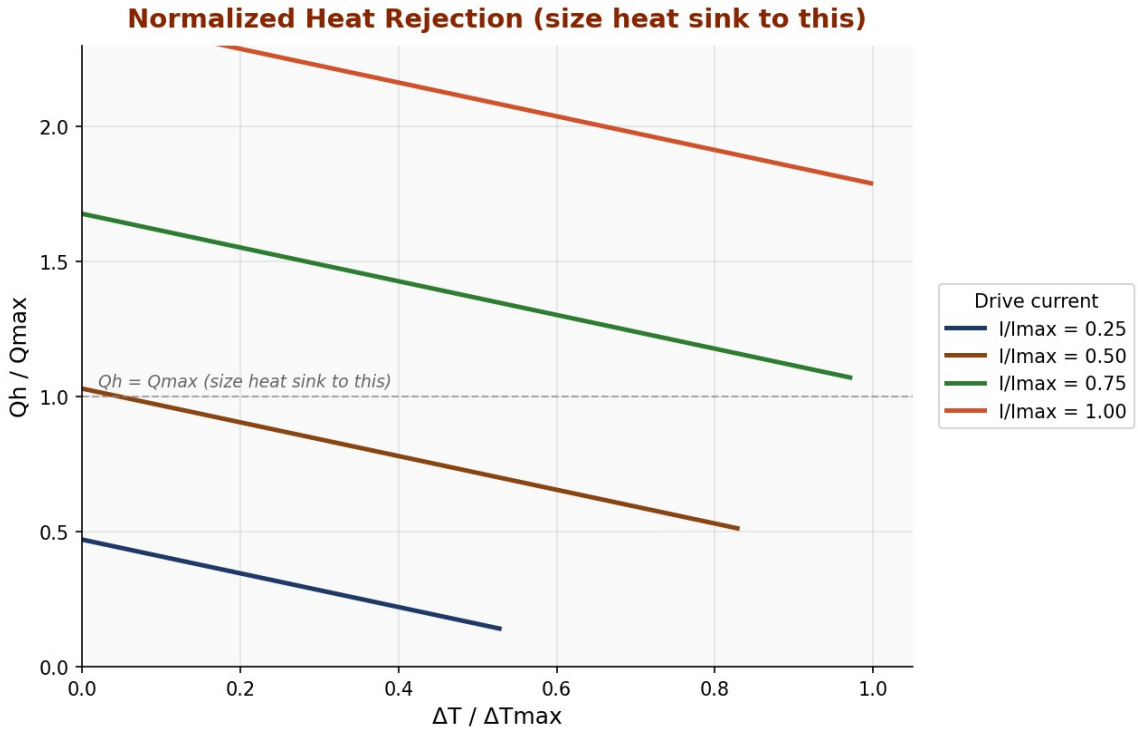

Figure 9: *Normalized heat rejection Qh/Q_{max}. The heat sink must handle Qh, not Qc — and at high I/Imax, Qh exceeds Q_{max} even though useful cooling (Qc/Q_{max}) is well under 1. The dashed line marks $Qh = Q_{max}$ for reference.*

Curve 6 — Electrical Input $Pin/(V_{max}\cdot I_{max})$ vs. $\Delta T/\Delta T_{max}$

Electrical input power normalized to the product of datasheet maximums. Pin rises with current and with ΔT (the Seebeck back-EMF α·ΔT grows the voltage). Combined with Curve 4 (COP) this lets you predict both the wall-power draw and the heat-sink load for any operating point — and it tells you the power-supply rating you need from the controller.

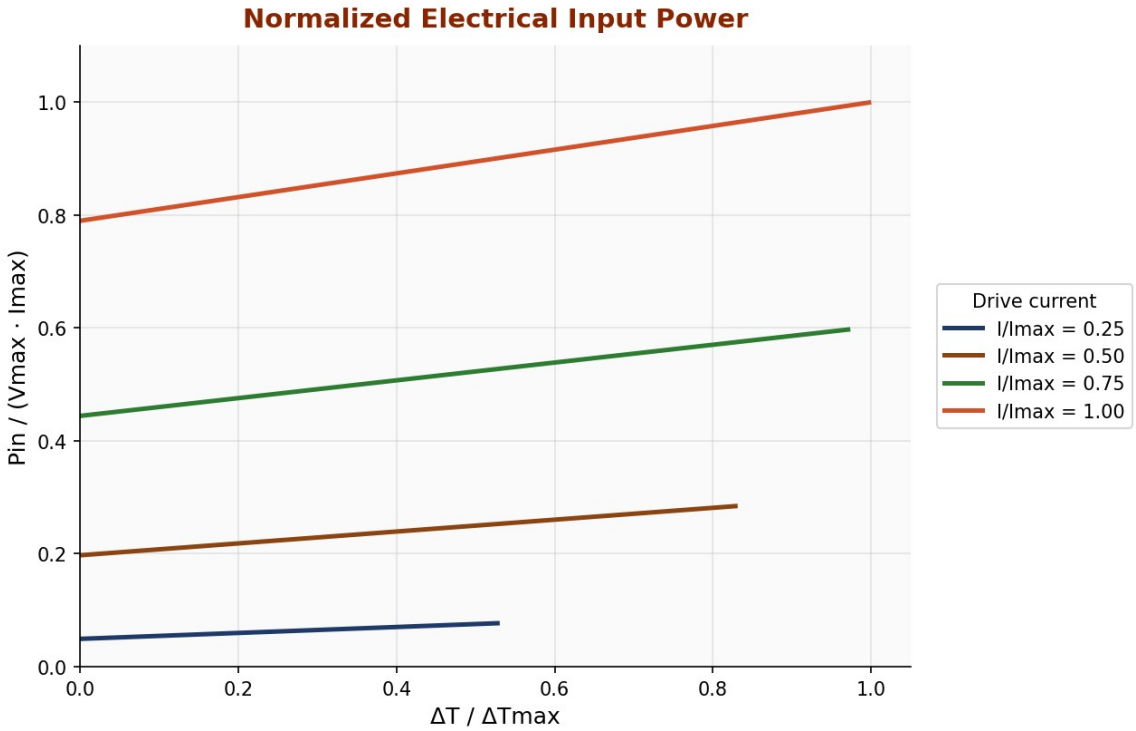

Figure 10: *Normalized electrical input power Pin/(V_{max}·I_{max}). Use this with Curve 5 (Qh) to set the controlle* ***r's power rating and the heat sink****'s thermal resistance — both downstream of how hard you drive the TEC module.*

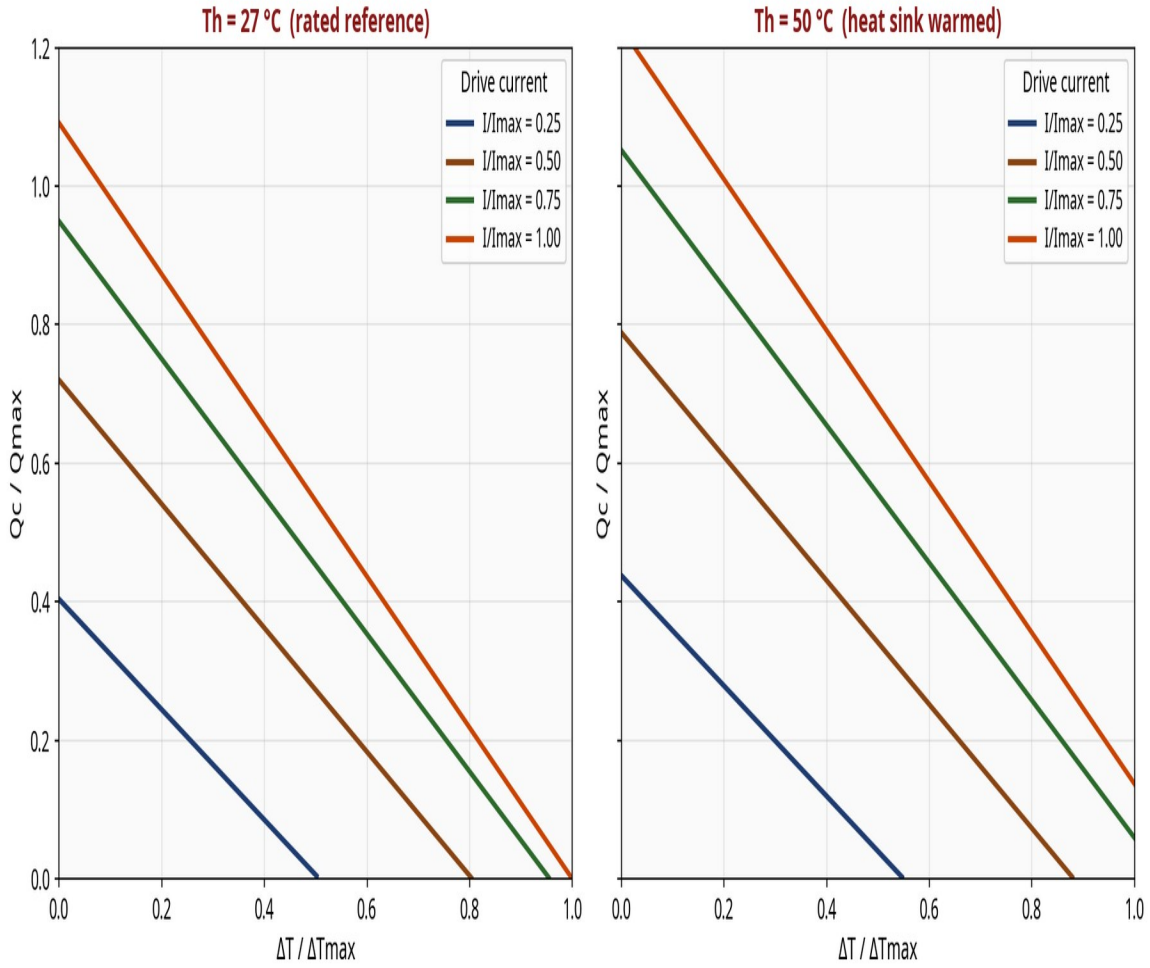

Figure 11: *Normalized cooling capacity Qc/Qmax vs. $\Delta T/\Delta T_{max}$ at two hot-side temperatures (T_h = 27 °C and T_h = 50 °C). Higher hot-side temperature shifts every constant-current curve outward — the same module pumps more useful cooling at warmer T_h.*

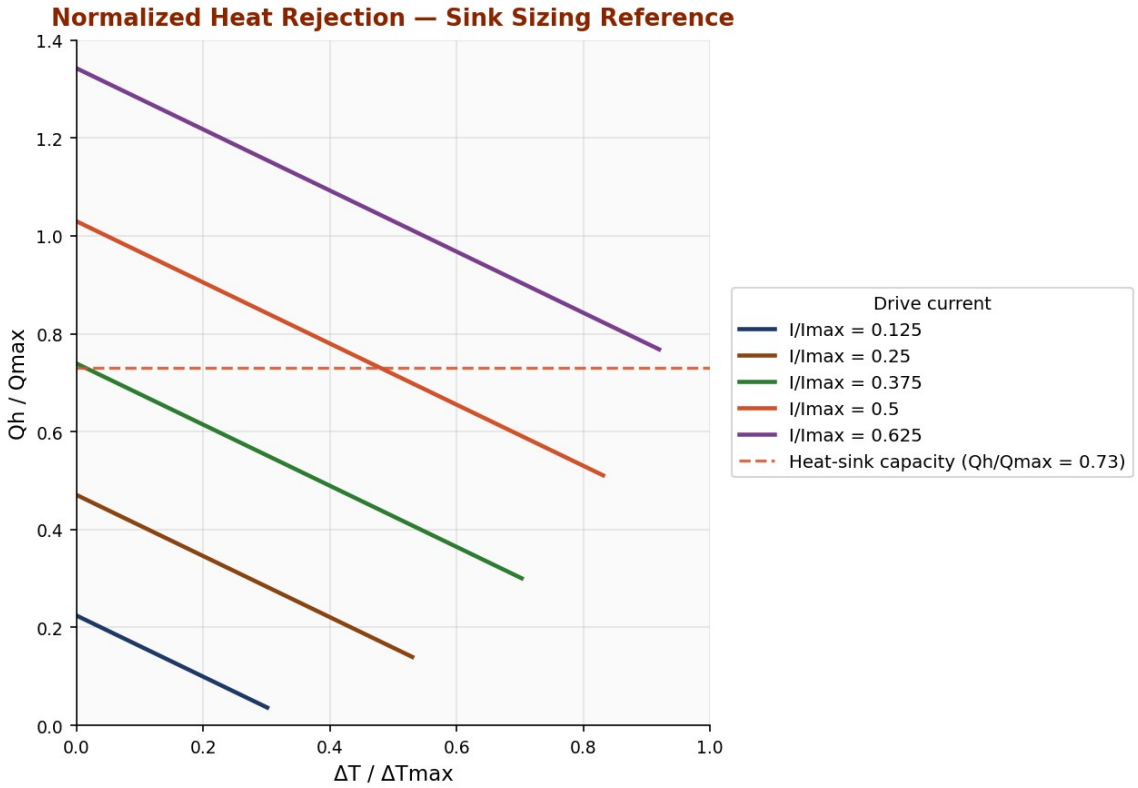

Figure 12: *Normalized heat rejection $Q_h/Qmax = (Qc + P_{in})/Qmax$ vs. $\Delta T/\Delta T_{max}$ at T_h = 27 °C, family from I/I_{max} = 0.125 to 0.625. The dashed line marks a representative heat-sink capacity at $Q_h/Qmax$ = 0.73; any operating curve above it means the sink is undersized at that ΔT and current.*

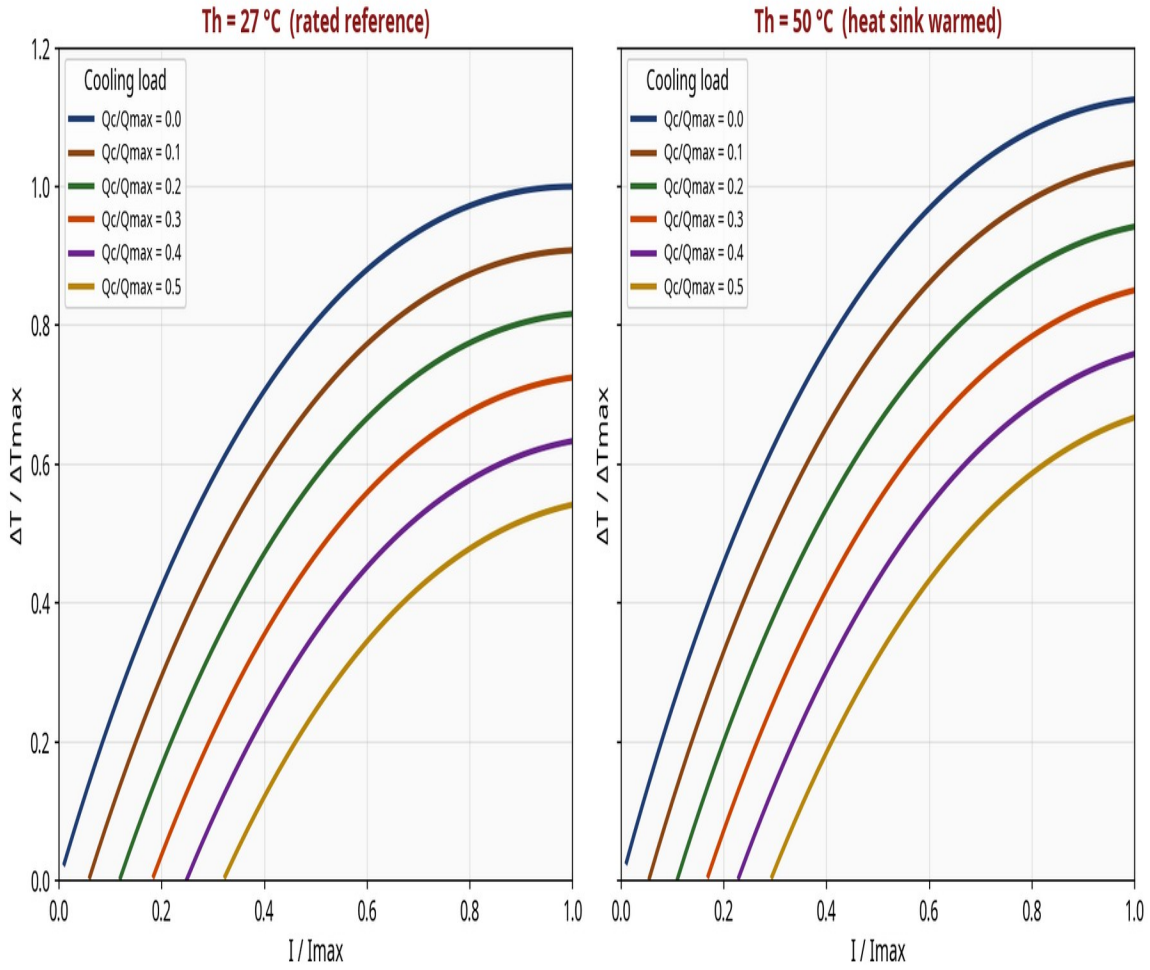

Figure 13: *$\Delta T/\Delta T_{max}$ achievable at constant cooling load Qc, as a function of I/I_{max} for Qc/Qmax = 0 (outer envelope) through 0.5. Each curve is an inverted parabola: low current → Peltier dominates → ΔT rises; past the peak (near I/I_{max} = 1.0) Joule heating overtakes and ΔT falls.*

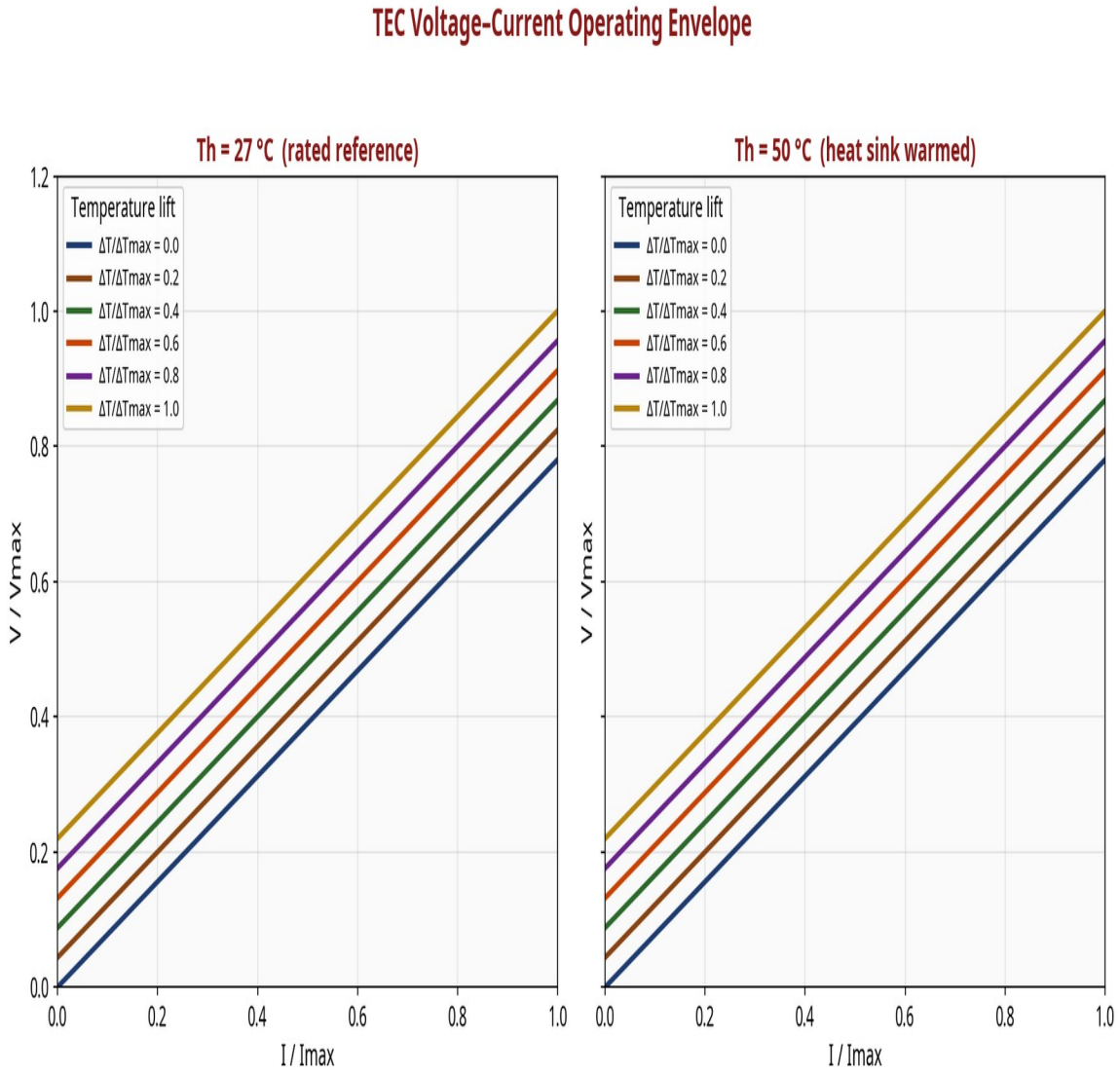

Figure 14: *TEC terminal voltage V/V_{max} vs. I/I_{max}, bracketed by the two boundary curves: $\Delta T = 0$ (lower curve, purely resistive: $V = I \cdot R$) and $Q_c = 0$ (upper curve, the TEC module is at its maximum ΔT for that current). Use this to size the controller's voltage rating.*

Curves 1–6 all assume the datasheet reference Th = 27 °C. Real systems run at whatever hot-side temperature the heat sink delivers — and that temperature reshapes ΔT_{max} in a way most engineers find surprising. The next subsection derives why, plots ΔT_{max} for the full Th range, and gives you a table to scale any ATI module's ΔT_{max} to your actual hot-side temperature.

5.5 Why ΔT_{max} Depends on Hot-Side Temperature — Advanced Theory

The headline result: ΔTmax is not a fixed constant. It grows with the hot-side temperature. A module rated for ΔTmax = 66 °C at Th = 27 °C reaches about 76 °C

at Th = 50 °C and over 96 °C at Th = 100 °C. The hardware has not changed; the physics simply favors warmer operation. This subsection derives the result, gives the closed-form expression, and provides a numerical table for engineering use.

Note: the datasheet rates ΔTmax = 66 °C (rounded); the exact closed-form expression ½·Z·Tc,ref² yields ≈ 66 °C at Th = 300 K using Z = 2.41 × 10^{-3} K^{-1}. The §5.5.4 prediction table uses the closed-form value for internal consistency; all other sections use the datasheet value of 66 °C.

Design caution: A larger theoretical ΔTmax at elevated Th does not mean the system should be run hot. High Th increases hot-side rejection burden, raises absolute Tc, and accelerates solder/interconnect fatigue. For most precision and long-life systems, target Th ≤ 50 °C even if the theoretical ΔTmax curve appears larger at elevated Th.

Important: At Th ≥ 80 °C, standard S-series modules approach the BiSn solder melting point (138 °C). For sustained operation above Th = 80 °C, specify the H-series variant (e.g., ATE1-127-8AH (www.analogtechnologies.com/tec-module)) which uses high-temperature SnSb solder (Tmelt 232 °C), rated to Th = 200 °C. Standard modules may suffer solder creep and premature open-circuit failure at elevated hot-side temperatures.

5.5.1 Deriving ΔT_{max} from First Principles

Set Qc = 0 in the energy balance (the defining condition of ΔT_{max} — module at full span, zero useful load) and solve for ΔT as a function of I:

$$\Delta T_{max}(I) = [\alpha \cdot Tc \cdot I - \tfrac{1}{2} \cdot R \cdot I^2] / K$$

This is a parabola in I. Differentiate with respect to I and set the derivative to zero to find the current that maximizes ΔT:

$$I_{opt\_\Delta T} = \alpha \cdot Tc / R$$

Substitute back into the parabola:

$$\Delta T_{max} = \tfrac{1}{2} \cdot (\alpha^2 / RK) \cdot Tc^2 = \tfrac{1}{2} \cdot Z \cdot Tc^2$$

This is the master equation. The maximum temperature difference scales with the square of the cold-side absolute temperature, with a proportionality constant ½·Z set by the thermoelectric figure of merit. For bismuth telluride at room temperature, Z ≈ 2.4 × 10^{-3} K^{-1}, and the dimensionless figure of merit ZT (multiplying by absolute temperature) is the universal metric for thermoelectric material quality. Conventional Bi_2Te_3 delivers ZT ≈ 1 at room temperature.

5.5.2 The Freight-Train Analogy

Engineers control Th (via the heat sink), but the master equation is in Tc. Because ΔT = Th − Tc, raising Th also raises Tc at the maximum-ΔT operating point. And

since ΔT_{max} scales with Tc^2, the effect compounds: higher Th → higher Tc → more Peltier heat per amp → larger ΔT_{max}.

Picture the TEC as a freight railroad running between two loading docks. The number of cars on the train is the drive current I. The cargo per car is the Peltier load per coulomb, q = α·Tc. The colder the loading dock, the smaller the cargo each car can hold.

Cold ambient (Th = 0 °C): the cold dock sits at about −58 °C (215 K). Each rail car holds only 215·α joules per coulomb. Modest span: $\Delta T_{max} \approx 58$ °C. Warm ambient (Th = 100 °C): the cold dock sits at about +4 °C (277 K). Each rail car holds 277·α joules — 29% more cargo per car. Same train, same engine, same parasitic enemies, but each trip moves enough extra heat to push the span to $\Delta T_{max} \approx 96$ °C. The two effects (larger cargo per car AND extra cargo helping to overcome the parasitic losses) compound to give the Tc^2 dependence.

5.5.3 The Closed-Form Result in Th

For engineering use we want ΔT_{max} as a function of Th (which the heat sink determines). Substitute $Tc = Th - \Delta T_{max}$ into the master equation and solve the resulting quadratic:

$$\Delta T_{max}(Th) = Th + 1/Z - \sqrt{(2 \cdot Th/Z + 1/Z^2)}$$

This is the exact closed-form solution. A simplified approximation $\Delta T_{max} \approx \frac{1}{2} \cdot Z \cdot Th^2$ is sometimes seen, but it overestimates substantially for real Bi_2Te_3 because Z·Th is of order 1, not $\ll 1$. Always use the exact form for quantitative work — Curve 7 below plots it for the full operating range.

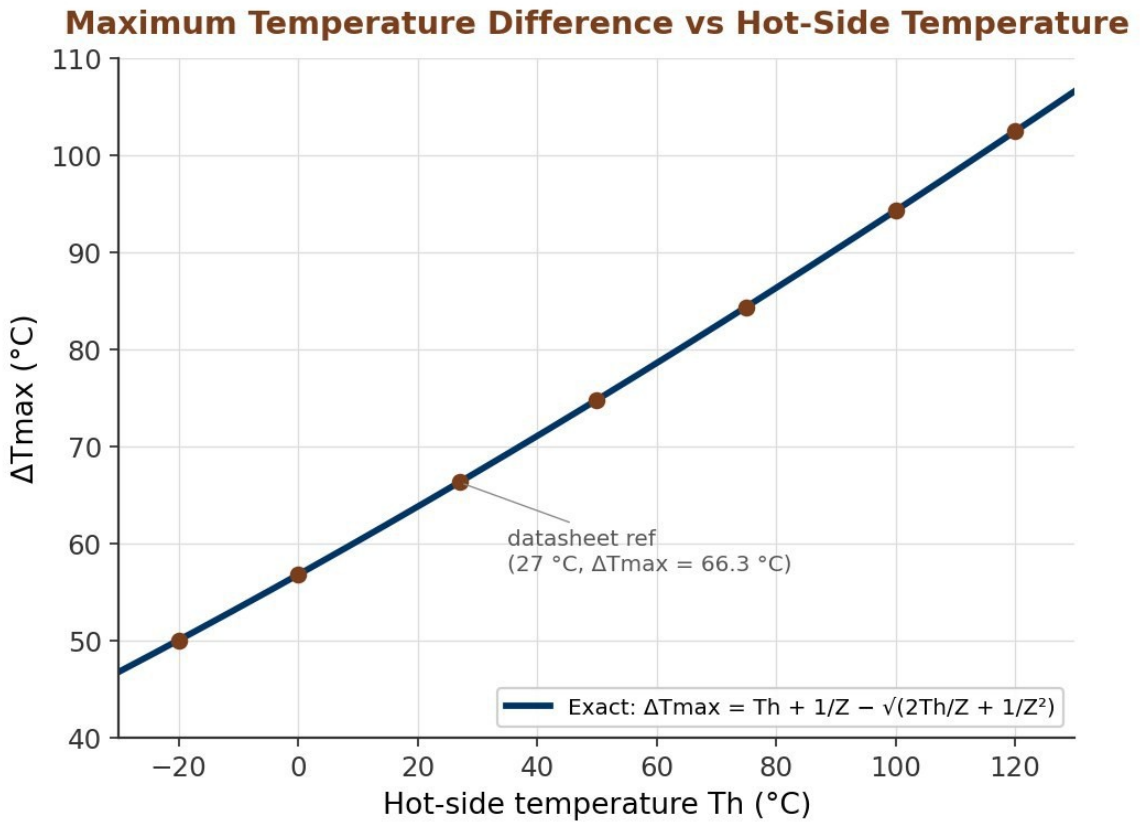

Figure 15: *Curve 7 — ΔT_{max} in °C as a function of hot-side temperature Th in °C, from the exact closed-form expression. The datasheet reference point (27 °C, 66 °C) is marked. Multiply the ratio $\Delta T_{max}(Th)/\Delta T_{max}(27\ °C)$ by your module's datasheet ΔT_{max} to predict the achievable span at any hot-side temperature.*

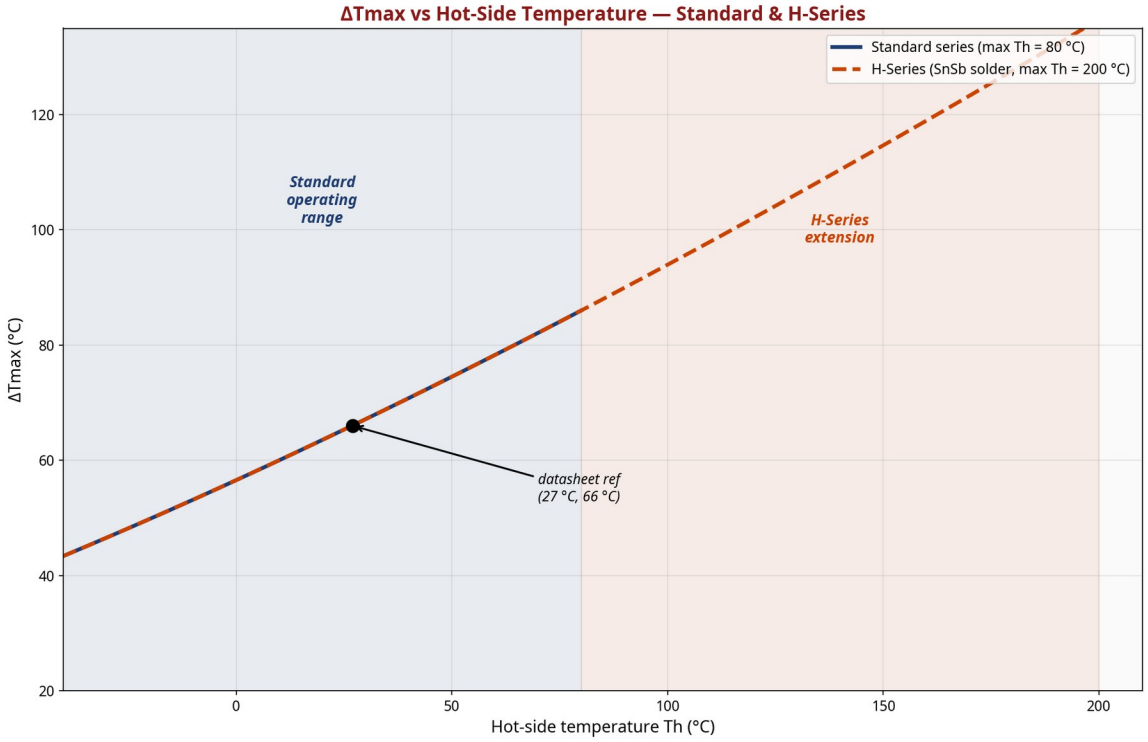

Figure 16: *ΔT_{max} vs hot-side temperature T_h for the standard* ATE1-127 series (5/8/15 A overlap) and the H-series (5/8 A H-class overlap). The standard series tops out near ambient; the H-series uses SnSb solder (Tmelt 232 °C) and pushes operation up to T_h = 200 °C.

5.5.4 Numerical Predictions

Note: This table uses Z = 2.41 × 10^{-3} K^{-1} (consistent with ATE1-127 datasheet ΔTmax = 66 °C at Th = 27 °C). The canonical value Z = 2.41 × 10^{-3} K^{-1} in §5.2 applies at Th,ref = 300 K:

Th (°C)	Th (K)	Tc (K)	ΔT_{max} (°C)	ΔT_{max} / ΔT_{max}ref	I_{opt} / I_{max}
−20	253	202	51.1	0.755	0.87
0	273	215	57.9	0.857	0.93
27	300	233	66.0	1.000 (ref)	1.00
50	323	247	76.2	1.128	1.06
75	348	262	85.9	1.271	1.13
100	373	277	96.0	1.420	1.19
120	393	289	104.3	1.543	1.24

How to use the table: multiply the $\Delta T_{max}/\Delta T_{max}$ref ratio by your module's datasheet ΔT_{max} to predict the span at your actual Th. Multiply I/I_{max} by the datasheet I_{max} to find the drive current that achieves that maximum span at that Th.

Important: Rows above Th = 85 °C apply to H-series (SnSb solder) modules only. Standard BiSn-solder modules must not be operated at Th > 85 °C. For standard modules, target Th ≤ 50 °C for best lifetime and keep Th < 85 °C as an absolute maximum.

5.5.5 Two Different Optimum Currents

A critical distinction often missed: there are two optimum currents depending on what you are optimizing.

Goal	Optimum current	Typical I/I_{max}	Use when
Maximum ΔT (deepest cooling)	$I_{opt\_\Delta T} = \alpha \cdot T_c / R$	0.87–1.24	You need the largest possible span
Maximum COP (best efficiency)	$I_{opt,COP} = \alpha \cdot \Delta T / [R \cdot (\gamma - 1)]$	0.20–0.35	You want maximum cooling per watt

For most precision applications (laser diodes, detectors, medical instruments), operate at the COP-optimum current. Reserve the max-ΔT current for applications where achieving the deepest possible cold-side temperature is the overriding priority — typically deep-cooled detectors or test chambers below −40 °C.

ΔT_{max} tells you the largest span the TEC module can sustain; Th tells you where that span starts. The closing subsection completes the loop — how to design the hot-side thermal network so Th actually lands where the curves assume it does.

5.6 The Thermal Network — Designing the Hot Side

The most common reason TEC systems fail in the field is not a bad module — it is an inadequate hot side. The heat sink must reject ALL of Qh = Qc + Pin (Curve 5 in §5.4), not just the useful cooling load Qc. This subsection gives the equations and the design discipline to never make that mistake.

$\Delta T = Q \times R_{th}$

5.6.1 Thermal-Network Master Equation

ΔT = Q × Rth

This single Ohm's-law analogy is the foundation for every thermal resistance calculation in this section. Q is the heat flow in watts (for TEC hot-side sizing, Q = Qh = Qc + Pin), Rth is the thermal resistance in °C/W, and ΔT is the resulting temperature difference in °C. Every component in the thermal path — TIM layers, heat-sink base, fins, and convection boundary — adds its own Rth in series, just as electrical resistors add in series.

5.6.2 The Hot-Side Temperature Equation

$$\mathbf{Th = T_{amb} + Qh \times (R_{TIM} + R_{hs})}$$

Here T_{amb} is ambient air (or coolant) temperature, Qh = Qc + Pin is the total heat the TEC dumps to the hot side (read directly off Curve 5 in 5.4 and multiply by Q_{max}), R_{TIM} is the thermal resistance of the thermal interface material between TEC and heat sink (typically 0.10–0.30 °C/W for a thin layer of quality grease), and R_{hs} is the heat-sink-to-ambient thermal resistance.

The #1 TEC design mistake: sizing the heat sink for Qc instead of Qh. The TEC adds its own electrical dissipation to the heat that must be rejected. For COP = 2, Qh = 1.5·Qc; for COP = 1, Qh = 2·Qc; for COP = 0.5, Qh = 3·Qc. Always go look at Curve 5 of 5.4 and Curve 6 of 5.4 before specifying the heat sink.

5.6.3 Maximum Allowable Heat-Sink Resistance

Rearrange to solve for the heat sink:

$$\mathbf{R_{hs} \leq (T_{h,max} - T_{amb}) / Qh - R_{TIM}}$$

Target Th ≤ 50 °C for most applications. Although §5.5 shows that the intrinsic no-load ΔTmax grows with Th, hitting a fixed cold-side target gets harder as Th rises because the required ΔT (= Th − Tc) grows faster than the achievable ΔTmax. Higher Th also increases hot-side rejection burden and accelerates solder/interconnect fatigue and shortens lifetime via accelerated solder creep. IMPORTANT: Although theoretical ΔTmax increases with Th, a warmer hot side almost always makes the real system harder to cool because heat-sink margin decreases, solder stress increases, and lifetime decreases. Do not intentionally run the hot side hotter to improve performance. Although the intrinsic no-load ΔTmax of a Bi_2Te_3 module increases with absolute Th, a hotter hot side usually makes the system design worse: it raises the absolute cold-side starting point, increases Qh, reduces margin to the desired Tc, and accelerates solder/interconnect fatigue. For most precision and long-life systems, target Th

≤ 50 °C even if the theoretical ΔTmax curve appears larger at elevated Th.

CAUTION: Do not misread this relationship. While intrinsic ΔTmax rises with Th, achieving a given cold-side target temperature generally becomes harder as Th increases — because the absolute starting point rises, the Qh burden on the heat sink grows, and lifetime margin shrinks.

5.6.4 Heat-Sink Options by Cooling Method

Cooling method	Typical R_{hs} (°C/W)	Best for	Notes
Natural convection (passive fins)	2–10	Qh < 5 W	Silent, no moving parts, large volume
Forced air (fan + fins)	0.3–2	Qh = 5–100 W	Compact, cost-effective, some noise
Liquid cold plate	0.05–0.3	Qh > 50 W	Excellent performance, needs pump
TEC on chiller (cascade)	< 0.05	Extreme precision	Maximum performance, highest complexity

5.6.5 Design Margin

Always add 20–30% margin to the calculated R_{hs} requirement.

Dust accumulation on fins, fan-bearing wear, elevated summer ambients, enclosed-cabinet operation, and manufacturing tolerances all degrade real-world performance. A little extra thermal margin today prevents field failures tomorrow.

Quick answer: *Section 5 takeaway: four datasheet numbers (Qmax, Vmax, Imax, ΔT_{max}) define the TEC module physics through α, R, K, Z. Operate in the Goldilocks zone I/I_{max} = 0.20–0.35 (Curve 4) for best COP. ΔT_{max} grows with Th per $\Delta T_{max}(Th) = Th + 1/Z - \sqrt{(2Th/Z + 1/Z^2)}$ (Curve 7). Size the heat sink for Qh, not Qc, and target Th ≤ 50 °C.*

PART II — DECISION

When to Choose a TEC and How to Specify One

6. When to Choose a TEC — Comparison with Fan and Compressor Cooling

With the physics and performance reference from Part I in hand, the comparison with other cooling technologies becomes precise rather than hand-wavy. To understand where a TEC fits in the thermal-management landscape, imagine three characters managing heat in a busy electronics laboratory.

The TEC — Precision Solid-State Heat Pump

The TEC is a calm, well-mannered robot of semiconductor layers. It silently directs invisible electron "butlers" to ferry heat packets one-way from the cold face to the hot face. It is precise, reliable, makes no complaints, and works in any orientation — upside down, sideways, in zero gravity. It needs a good controller and a properly sized heat sink. It is not the strongest lifter in the room, but for precision work in tight spaces, nothing else comes close.

Forced-Air Cooling — Simple but Limited

The fan is boisterous and dusty with a big spinning mouth. It pushes ambient air around vigorously, but can only reject heat into that air — it can never cool below ambient temperature. It collects dust, wears out at the bearings, and vibrates enough to disturb sensitive optical or mechanical systems. For bulk air movement at low cost, unbeatable. For precision, silence, or sub-ambient cooling, it is simply the wrong tool.

Vapor-Compression — Powerful but Complex

The compressor is complicated and noisy — pipes, valves, evaporator, condenser, and a grumpy face. It does heavy lifting efficiently for large thermal loads: buildings, refrigerators, industrial chillers. But it leaks occasionally, vibrates, requires periodic maintenance, uses refrigerants with environmental concerns (ODP, GWP), takes time to start up, and cannot easily be miniaturized below about 50 W of cooling capacity. Powerful for big jobs; overkill and finicky for precision small-scale work.

6.1 Head-to-Head Comparison

Criterion	TEC (Thermoelectric)	Fan (Forced Air)	Compressor (Vapor)
Sub-ambient cooling	Yes — up to ~70 °C below	No — ambient is the floor	Yes — large ΔT possible

Criterion	TEC (Thermoelectric)	Fan (Forced Air)	Compressor (Vapor)
	Th		
Moving parts	None (solid state)	Bearings, blades	Compressor, valves, fans
Acoustic noise	0 dBA	20–50 dBA	40–70 dBA
Vibration	None	Bearing-induced	Significant
Refrigerant	None	None	Yes (R-134a, R-410 A, etc.)
Temperature precision	±0.001–0.01 °C	±5 °C typical	±0.5–1 °C
Bidirectional (heat/cool)	Yes (reverse current)	No	Rarely (heat-pump mode)
Compact (10 W cooling)	40×40×4 mm module	80×80×25 mm fan + sink	150×100×100 mm minimum
Orientation sensitivity	None	Reduced if airflow blocked	Gravity-dependent (oil)
Startup time	Seconds	Instant air, slow thermal	Minutes
COP for the cooling job	0.3–4 (depends on ΔT, I/I_{max})	Not applicable	2–6 for large loads
Maintenance	None — sealed for life	Bearings, dust cleaning	Refrigerant recharge
Environmental impact	None (no refrigerant)	Energy use only	GWP from refrigerant leaks
Best for	Precision, silence, compact, sub-ambient, bidirectional	Bulk above-ambient air movement	Large industrial cooling, HVAC

6.2 Advantages of Thermoelectric Cooling

- **Solid-state reliability** — No moving parts, no wear-out under steady-state operation. ATI modules achieve a predicted MTBF exceeding 200,000 hours (from accelerated-life testing) (>22 years) of continuous service in laser diode and detector applications under steady-state thermal conditions.
- **Silent and vibration-free** — Zero acoustic noise, zero mechanical vibration. Essential for audio measurement, medical imaging, optical-table experiments, and consumer devices where silence is a premium.
- **Millikelvin precision** — **With ATI's precision TEC controllers (ATI's proprietary auto-PID compensation network (patent pending; see TEC controller datasheets for details)), temperature stability better than ±0.001 °C has been demonstrated in laboratory environments, eliminating the manual loop tuning that frustrates non-specialists.**
- **Compact and lightweight** — A 40×40×4 mm module delivering 30+ W of cooling fits where no compressor could ever go: handheld instruments, PCB-level integration, miniaturized optical assemblies.
- **Environmentally clean** — No refrigerants. No ozone-depletion potential. No global-warming-potential gases to leak. As regulations on fluorinated gases tighten, solid-state cooling becomes increasingly attractive for compliance.
- **Bidirectional operation** — Reversing current reverses the heat-pumping direction. One module both cools below ambient AND heats above ambient — uniquely valuable for thermal cycling, environmental testing, and any setpoint near ambient.
- **Orientation-independent** — No working fluid that depends on gravity. Works upside down, sideways, in microgravity — enables aerospace, automotive, and portable use.
- **Fast response** — Thermal time constant of 10–60 s depending on load mass. A well-tuned TEC system reaches setpoint in seconds — far faster than a compressor that must ramp up, circulate refrigerant, and stabilize.

6.3 Disadvantages — A Candid Comparison with Compressor Systems

TECs are not magic. Three honest tradeoffs deserve attention, especially when comparing with vapor-compression chillers.

- **Lower COP for large loads** — Vapor-compression systems achieve COP of 2 to 6 for loads above ≈100 W; a TEC typically operates at COP 0.3 to 1.5 (and up to ≈4 at very small ΔT in cooling mode; when used as an active heat spreader at zero or negative ΔT (see §5.3.4 and Example C), COP can exceed 10). For bulk cooling of large volumes, a compressor consumes less wall power per watt removed.
- **Limited single-stage ΔT** — A single-stage Bi_2Te_3 TEC reaches $\Delta T_{max} \approx$ 68–75 °C at Th = 27 °C; compressors can produce much larger spans with intermediate-pressure stages. For ΔT > 80 °C, multi-stage cascaded TEC modules or a hybrid TEC-on-chiller architecture is required.
- **Hot-side heat rejection is mandatory** — The TEC adds its own electrical dissipation to the heat that must be rejected (Qh = Qc + Pin, see Curve 5 in Section 5.4). The heat sink is therefore always larger than for a passive design pulling out the same Qc. An undersized hot side is the single most common cause of TEC field failure.

6.4 The Right Question to Ask

Choose a compressor for whole-room cooling above ≈200 W of load where precision is not critical. Choose a TEC any time you need precision (better than ±0.1 °C), silence, compactness, sub-ambient operation, or bidirectional control — and the cooling load is below about 200 W. The two technologies are complements, not competitors. ATI's most demanding customers run TECs on top of compressor-cooled cold plates: the compressor handles bulk heat lift, the TEC delivers the final millikelvin of precision.

Quick answer: *TEC: precision, silence, compactness, sub-ambient, bidirectional, but lower COP than a compressor for large loads. Compressor: high COP for bulk cooling, but noisy, vibrating, refrigerant-bearing, and bulky. The two technologies are complementary.*

6.5 Three Ways to Design a TEC System

When engineers sit down to select a thermoelectric cooler and design the surrounding thermal system, they typically have one of three primary objectives in mind. The mathematical approach changes drastically depending on which of these three goals drives the design:

1. COP-Optimized Design (Minimum Power) — Maximizing efficiency for battery-powered devices or systems with strict thermal dissipation limits.

2. Minimum-Size Design (Minimum Footprint) — Shrinking the TEC to the absolute smallest physical size capable of handling the load, typically for compact opto-electronics.

3. Maximum-ΔT Design (Maximum Cooling) — Driving the cold side to the lowest possible temperature, regardless of efficiency or size, often used for IR detectors or cryogenic pre-cooling.

The previous section detailed the exact physics of the COP-optimized method. Below, we summarize all three approaches, provide the governing formulas, and walk through practical examples for each.

6.5.1 Method 1: COP-Optimized Design (Minimum Power)

Goal: Achieve the required cooling load (Qc) and temperature differential (ΔT) while consuming the absolute minimum electrical power. This minimizes the heat rejected to the ambient (Qh), which in turn shrinks the required heat sink and fan.

As derived in Section 5.3, the optimum operating current is roughly 30% of Imax, and the module must be significantly oversized ($Q_{max} \approx 5\times$ to $8\times$ Qc).

Key Design Formulas:

$$I_{opt} = (\alpha \cdot \Delta T) / [R \cdot (\gamma - 1)]$$

I_{opt}: Optimum current [A] | α: Seebeck coefficient [V/K] | R: Electrical resistance [Ω] | γ: Ioffe parameter

$$COP_{max} = (Tc / \Delta T) \cdot (\gamma - Th/Tc) / (\gamma + 1)$$

COP_{max}: Maximum Coefficient of Performance | Tc: Cold-side temp [K] | Th: Hot-side temp [K]

$$Qmax,min \approx Qc / (0.54 \cdot \theta + 0.034)$$

Qmax,min: Minimum datasheet Qmax required [W] | Qc: Cooling load [W] | θ: Normalized lift (ΔT/ΔTmax)

When to use it: Battery-powered instruments, dense enclosures where rejecting heat is difficult, or any system where operating cost/power dominates. For example, cooling a high-power AI accelerator or stabilizing a telecom DFB laser in a sealed chassis.

6.5.2 Method 2: Minimum-Size Design (Minimum Footprint)

Goal: Find the absolute smallest TEC module that can just barely achieve the required cold-side temperature (Tc) at the worst-case ambient temperature (Ta), completely disregarding efficiency (COP).

To extract the maximum possible cooling capacity from a given footprint, the TEC must be driven at its maximum current ($I = I_{max}$). At this operating point, the cooling capacity decreases linearly with the temperature differential.

Key Design Formulas:

$$Q_{max,min} = Q_c / (1 - \Delta T / \Delta T_{max})$$ **[First-pass screening only — valid for quick rejection of undersized modules. Final selection must use the normalized curves or full energy balance including Th rise.]**

$Q_{max,min}$: Minimum datasheet Q_{max} required [W] | Q_c: Cooling load [W] | ΔT: Temperature diff [K] | ΔT_{max}: Max diff [K]

Note that the formula above assumes the hot side of the TEC is held perfectly at the datasheet reference temperature (typically 27 °C). In reality, operating at I_{max} generates massive Joule heating, requiring an excellent heat sink. If the heat sink allows Th to rise significantly, the required Q_{max} increases:

[Approximate screening formula — use only to reject obviously undersized modules; verify final selection with normalized performance curves.]

$$Q_{max,min} \approx Q_c / (1 - (\Delta T / \Delta T_{max}) \cdot (T_h / 300))$$

T_h: Actual hot-side temperature [K] | 300: Reference temperature [K]

When to use it: Ultra-compact opto-electronics, such as TO-can packages, butterfly packages, or miniature optical receivers where physical space is the absolute hard constraint. The ATE1-07 series (as small as 4×4 mm) and ATE1-17 series are frequently used in this regime.

Worked Example: Minimum-Size Photodetector Cooling

Scenario: A miniature photodetector generates Q_c = 0.2 W of heat. It must be cooled to Tc = 0 °C in an ambient of Tamb = 25 °C. Space is severely limited, allowing only a tiny passive heat sink (R_{hs} = 20 K/W).

Module selection: We test the tiny ATE1-07-1AS (Q_{max} = 0.6 W, ΔT_{max} = 61.5 °C, I_{max} = 1.0 A, V_{max} = 0.8 V).

Using the self-consistent thermal loop equations ($T_h = T_{amb} + Q_h \cdot R_{hs}$):

• Operating at $I = I_{max}$ = 1.0 A

• The hot side rises to Th = 43.9 °C (due to the 20 K/W heat sink)

• The required ΔT is 43.9 °C - 0 °C = 43.9 °C

• The normalized lift θ = 43.9 / 61.5 = 0.714

• The available cooling capacity drops to Qc,avail = 0.22 W

Result: The module can provide 0.22 W of cooling, which just barely exceeds the 0.2 W load. The system works, but the efficiency is terrible (Pin = 0.75 W, COP = 0.27). This is the classic trade-off of minimum-size design: you sacrifice power to save space.

6.5.3 Method 3: Maximum-ΔT Design (Maximum Cooling)

Goal: Drive the cold side to the lowest possible absolute temperature. This is achieved by selecting a module with a massive Q_{max} capacity (so the active load Qc is a tiny fraction of its capability) and the highest available ΔT_{max}.

To achieve maximum ΔT, the module is driven at $I = I_{max}$. The actual achievable temperature differential is reduced from the datasheet ΔT_{max} by the presence of the active heat load Qc.

Key Design Formulas:

$$\Delta T_{actual} = \Delta T_{max} \cdot (1 - Qc / Q_{max})$$

ΔT_{actual}: Achievable temp diff [K] | ΔT_{max}: Datasheet max diff [K] | Qc: Load [W] | Q_{max}: Datasheet max cooling [W]

To reach cryogenic or deep-sub-ambient temperatures, the hot side (Th) must be aggressively cooled, typically using liquid cold plates or massive forced-air heat sinks, because the TEC will be pumping hundreds of watts of waste heat.

When to use it: Infrared (IR) detectors (MCT, InGaAs), low-noise scientific CCDs, and cryogenic pre-cooling stages. The ATE1-63 series (with ΔT_{max} up to 74.5 °C) and the high-power ATE1-127 series are ideal for this regime.

Worked Example: Deep Cooling an IR Detector

Scenario: An IR detector (Qc = 2.0 W) must be cooled as deeply as possible in a 25 °C ambient environment. A high-performance liquid cold plate (R_{hs} = 0.08 K/W) is available.

Module selection: We select the powerful ATE1-127-8AS (Qmax = 68.9 W, ΔTmax = 66.0 °C, Imax = 8.0 A, Vmax = 15.4 V). Notice how massively oversized Qmax is compared to the 2.0 W load.

Using the self-consistent thermal loop equations:

• Operating at I = I_{max} = 8.0 A

• The TEC consumes Pin = 128 W of electrical power

• Total heat rejected Qh = 130 W

• The liquid cold plate keeps the hot side at Th = 35.4 °C

• The module achieves an actual ΔT = 62.4 °C

Result: The cold side reaches Tc = -25.0 °C. The linear approximation formula predicts ΔT = 68.0 × (1 - 2.0/72.0) = 64.1 °C, which is reasonably close to the exact 62.4 °C value (the difference is due to Th being elevated above the 27 °C reference). The COP is a dismal 0.016, but the goal of deep cooling is successfully achieved.

6.5.4 Comparison of the Three Methods

Method	Primary Goal	Operating Current	Required Module Size	Typical COP	Best Applications
COP-Optimized	Minimum Power	$I_{opt} \approx 0.3 \times I_{max}$	Large (6–8× Qc)	1.5 to 4.0	Battery-powered, strict thermal limits
Minimum-Size	Minimum Footprint	I_{max}	Small (1.1–2× Qc)	0.3 to 0.8	Compact opto-electronics, TO-cans
Maximum-ΔT	Maximum Cooling	I_{max}	Largest available	0.1 to 0.5	IR detectors, deep cooling, cryo

7. How to Choose the Right TEC Module

Quick answer: Choose a module with Q_{max} >= 4-6x your actual cooling load, ensuring $\theta = \Delta T/\Delta T_{max}$ stays below 0.35 for good COP and long lifetime.

Selecting the correct module from a family of 49 variants is straightforward once you follow a systematic process. Everything in this section reduces to using the four datasheet numbers (5.1) together with the curve library (5.4) and the thermal network (5.6).

Important: Qmax is not the cooling load the module can remove at your target temperature. It is the zero-ΔT datasheet limit. Real available Qc must be read from the normalized performance curves or calculated from the energy balance using your actual ΔT and hot-side temperature.

7.1 The Golden Rule

Size your TEC so that Q_{max} is at least 2× — and ideally 3× to 4× — your actual cooling load Qc.

For most precision temperature-control systems, select a TEC module with Qmax about 4–6× the actual cooling load Qc. This rule keeps the TEC module in the Goldilocks zone (I/I_{max} = 0.20–0.35, Curve 4). A module operating at 25% of its capacity runs cooler, lasts longer, consumes less power per watt of cooling, and has thermal margin for worst-case ambient. The extra cost of a slightly larger module is trivial compared to system-level benefits. Use the ATI TEC Module Selection Guide to find the right module for your application.

Online tool: Use the ATI TEC Design Calculator (www.analogtechnologies.com/tec-calculator) to automate Steps 1–4 below. Enter your Qc, Tc, Tamb, and design target (balanced / min-size / max-efficiency) and the calculator returns the recommended module, operating point, and heat-sink budget in seconds — no manual iteration required.

7.2 The Five-Step Selection Flowchart

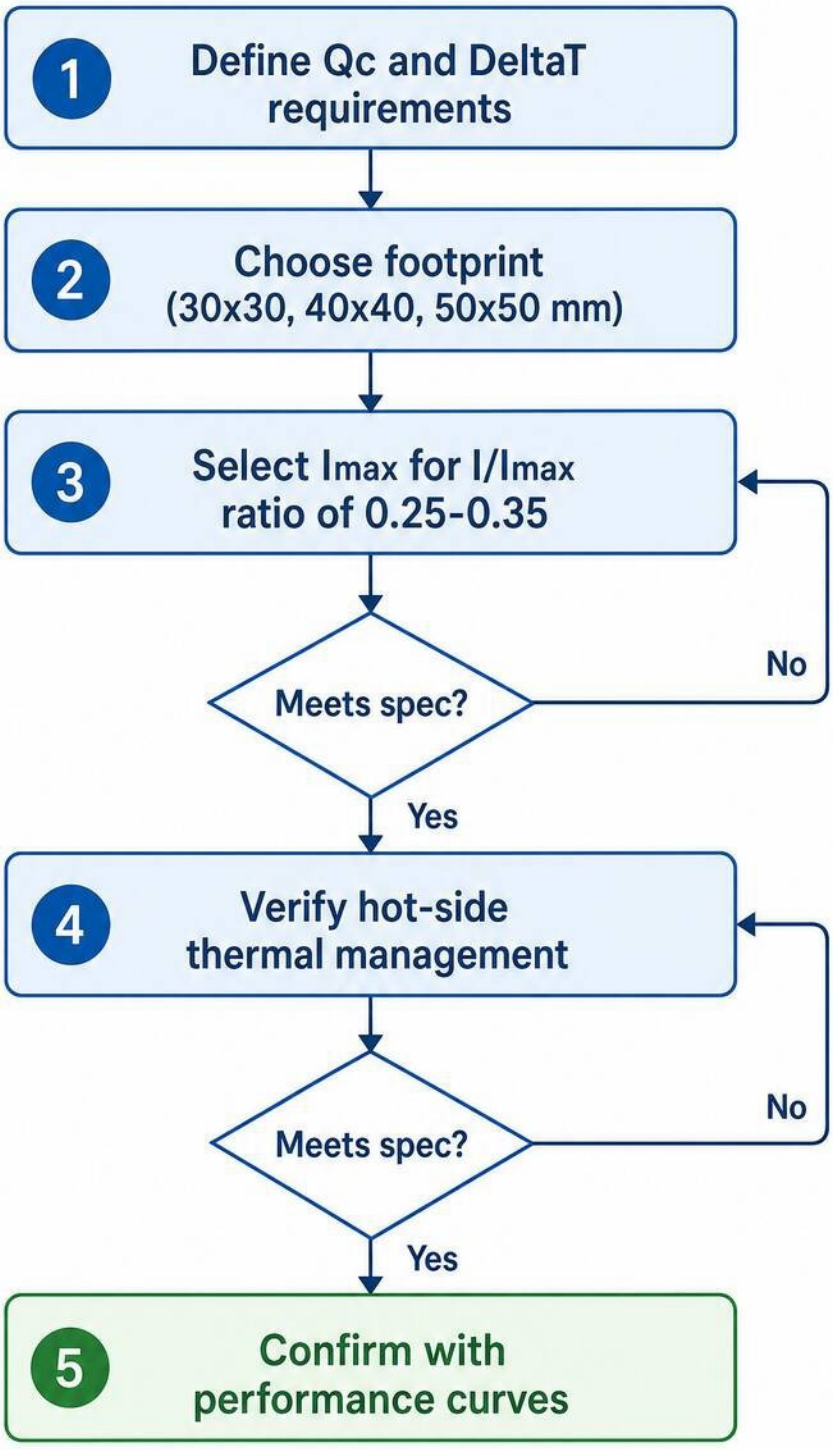

Figure 17: *Five-step selection flowchart. Iterate through requirements, footprint, current ratio, and hot-side management. If any check fails, move to a larger module or improve the heat sink.*

Step 1: Determine Qc. Sum every heat source on the cold side: device dissipation, conduction through mounting hardware, radiation from warm surroundings, and convection from exposed surfaces. For a laser diode, Qc is the electrical input minus the optical output. For a detector, it is the bias power plus any absorbed radiation.

Step 2: Determine required ΔT. ΔT = Th − Tc. Tc is your target cold-side temperature; Th depends on heat-sink performance. If you do not yet know Th, start with Th = T_{amb} + 10 °C and iterate using 5.6.

Step 3: Apply the oversizing rule: Qmax ≥ 2–3× Qc (compact/footprint-limited); 4–6× Qc (balanced precision); 6–8× Qc (maximum COP/battery) (>30 °C). As ΔT grows, more of the Peltier pumping is consumed by back-conduction.

Step 4: Filter the catalog. From the ATE1-127 series selection table below, pick modules whose Q_{max} exceeds the Step 3 requirement and whose ΔT_{max} exceeds Step 2. Filter by footprint to fit your mechanical envelope.

Step 5: Verify on the curves. Plot (Qc/Qmax, $\Delta T/\Delta T_{max}$) on Curve 1 in Section 5.4. Confirm the required current is below 40% of I_{max}. If it exceeds 50%, step up to the next-larger module.

7.3 Part-Number Decoder

Every ATE1-127 series part number follows the pattern ATE1-127-NN Y [S] [H], where NN is the I_{max} class (3 to 30 A), Y is A or B for footprint (A=smaller, B=larger within the current class), S indicates a perimeter epoxy seal for sub-dew-point operation, and H indicates SnSb high-temperature solder for Th up to 200 °C. Example: ATE1-127-10BSH is a 10 A class module on the 50×50 mm footprint, sealed, with high-temperature solder.

7.4 Quick-Reference Selection Table

Heat load Qc	Recommended Q_{max}	Suggested ATE1-127 modules	Footprint / θ Range
1–5 W	10–20 W	ATE1-127-3AS	30×30 mm / θ 0.15–0.40
5–15 W	20–43 W	ATE1-127-4AS, -5AS	30×30 mm / θ 0.15–0.35
15–25 W	43–60 W	ATE1-127-5AS,	30×30 or 40×40

Heat load Qc	Recommended Q_{max}	Suggested ATE1-127 modules	Footprint / θ Range
		-6AS, -7AS	mm / θ 0.15–0.30
25–40 W	60–85 W	ATE1-127-7AS, -8AS, -9AS	40×40 mm / θ 0.15–0.30
40–70 W	85–150 W	ATE1-127-10AS, -12BS	40×40 or 50×50 mm / θ 0.15–0.30
70–130 W	150–252 W	ATE1-127-15BS, -18AS, -30AS	50×50 mm / θ 0.15–0.30

Note: This table is a first-pass selection guide for balanced precision designs. Final module choice must be verified using the required ΔT, normalized performance curves, hot-side heat-sink resistance, mechanical footprint, and controller current rating. A 10 W load at ΔT = 5 °C and a 10 W load at ΔT = 45 °C require very different modules.

Quick answer: Apply Qmax ≥ 2–3× Qc (compact/footprint-limited); 4–6× Qc (balanced precision); 6–8× Qc (maximum COP/battery), then follow the five-step flowchart; choose H-series if Th may exceed 85 °C and S (sealed) if Tc may go below the dew point. View all variants with full specifications at .analogtechnologies.com/tec-module

7.5 Beyond the ATE1-127 — Choosing the Right TEC Series

While the ATE1-127 series (127 thermoelectric couples) dominates high-power applications such as cold plates, PCR thermal cyclers, and AI accelerator cooling, many precision applications require smaller, lower-power modules with footprints matched to the device being cooled. ATI manufactures a complete family of TEC modules spanning 7 to 127 couples, each optimized for a specific class of thermal load. Choosing the correct series eliminates wasted electrical power, minimizes footprint, and maximizes COP.

Quick answer: Match the TEC footprint to your device. Use ATE1-07 for TO-can lasers (4–8 mm), ATE1-17 for DFB lasers and small detectors (6–12 mm), ATE1-49 for CCD/CMOS imagers (20–25 mm), ATE1-63 for deep-cooling applications

requiring ΔT_{max} > 74 °C, ATE1-71 for large-area detectors (23–30 mm), and ATE1-127 for high-power loads (30–40 mm).

7.5.1 ATI TEC Module Family — Selection Guide

Series	Couples	Recommended Model	Q_{max} (W)	ΔT_{max} (°C)	Footprint (mm)
ATE1-07	7	ATE1-07-3AS	1.7	67	8 × 8
ATE1-17	17	ATE1-17-3AS	4.2	74.5	12 × 12
ATE1-49	49	ATE1-49-4AS	16.8	63	20 × 20
ATE1-63	63	ATE1-63-3.55AS	18.8	74.5	15 × 15
ATE1-71	71	ATE1-71-3AS	15.8	63	23 × 23
ATE1-127	127	ATE1-127-5AS	43.0	67	30 × 30

Table 1: ATI TEC module family — recommended models by application class. All models shown are sealed (S suffix) for moisture protection. Visit the complete selection guide for all variants.

7.5 When to Use Multi-Stage (Cascaded) TECs

A single-stage Bi_2Te_3 TEC module reaches a maximum no-load temperature difference of approximately 66 °C (at Th = 27 °C). When the application requires a larger ΔT or must maintain significant cooling capacity at high ΔT, cascaded (multi-stage) designs become necessary.

Decision tree for single-stage vs. multi-stage:

Use single-stage when: (1) Required ΔT < 50 °C under load, (2) COP matters (cascading always reduces system COP), (3) Space is limited vertically (each stage adds 3–5 mm height), (4) Cost sensitivity is high (multi-stage modules cost 2–5× more than single-stage).

Consider two-stage when: (1) Required ΔT = 50–80 °C under load, (2) Cooling capacity at high ΔT must exceed 10–20% of Qmax, (3) The application can tolerate COP < 0.5, (4) Vertical space allows 8–12 mm total module height.

Consider three-stage when: (1) Required ΔT > 80 °C, (2) Detector cooling to −60 °C or below from room ambient, (3) COP is secondary to achieving the target temperature, (4) The system budget supports premium module costs.

Parasitic penalties of cascading: Each additional stage adds its own Joule heating and Fourier conduction losses to the stage below it. The upper stage must pump not only the application heat load but also the total dissipation of all stages above it. This cascading penalty means that a two-stage system typically achieves only 60–70% of the theoretical ΔT improvement, and a three-stage system achieves 50–60%. Always verify with the manufacturer's multi-stage performance curves rather than extrapolating from single-stage data.

ATI offers the ATE1-63 series for deep-cooling applications requiring ΔT > 60 °C in compact form factors. For custom multi-stage configurations, contact the applications engineering team.

7.5.2 Application-Specific Guidance

Telecom and Fiber Optics (ATE1-07, ATE1-17): Laser diodes in DWDM systems require wavelength stability of ±0.01 nm, which translates to temperature

stability of ±0.001 °C. The ATE1-07-3AS (8×8 mm) fits directly under a standard 14-pin butterfly package, while the ATE1-17-3AS (12×12 mm) accommodates larger DFB laser assemblies. Pair with the TEC5V4A-D controller for sub-millikelvin stability (laboratory conditions, matched controller, 10 kΩ NTC).

Imaging and Spectroscopy (ATE1-49, ATE1-71): CCD and InGaAs sensors require cooling 20–40 °C below ambient to reduce dark current by 10–100×. The ATE1-49-4AS (20×20 mm) matches standard 1-inch sensor formats, while the ATE1-71-3AS (23×23 mm) covers larger focal-plane arrays. These modules deliver 15–17 W of cooling capacity — sufficient for sensors dissipating 2–4 W with a 30 °C temperature differential.

Deep Cooling (ATE1-63): When your application demands ΔT > 60 °C in a single stage (e.g., cooling an IR detector to −40 °C from a +25 °C ambient), the ATE1-63-3.4AS delivers ΔT_{max} = 74.5 °C — the highest single-stage performance in the ATI lineup. Its compact 15×15 mm footprint and 18.8 W Q_{max} make it ideal for dew-point hygrometers, cooled IR photodiodes, and cryogenic sample stages. For even deeper cooling, stack two stages (contact ATI for custom assemblies).

High Power (ATE1-127): For thermal loads exceeding 10 W or footprints larger than 25 mm, the ATE1-127 series remains the workhorse. With 127 couples delivering up to 120 W of cooling capacity (ATE1-127-30AS), these modules handle AI accelerator hotspots, PCR thermal cycling, and industrial cold plates. Pair with the TEC18V15A controller for loads requiring more than 8 A of drive current. For even higher-power applications (>15 A or multi-stage assemblies), the TEC28V15A-D provides 28 V input capability.

7.5.3 Matching Controller to Module

Each TEC series has an optimal controller match based on current and voltage requirements. Using an oversized controller wastes board space and cost; an undersized controller clips the drive current and limits cooling.

TEC Series	Recommended Controller	Max Current	Key Feature
ATE1-07, ATE1-17	TEC5V4A-D	4 A	Ultra-low noise, DIP package, ±0.001 °C (laboratory, constant load, controlled

			ambient) stability
ATE1-23, ATE1-35	TEC14M5V5AS	5 A	Micro form factor (25×25 mm), SMD mounting
ATE1-49, ATE1-63	TEC14M12V8AS	8 A	12 V rail, handles high-Vmax modules
ATE1-71, ATE1-127 (≤8 A)	TEC14M12V8AS	8 A	Cost-effective for moderate loads
ATE1-127 (>8 A)	TEC18V15A-D	15 A	High-power, 18 V input, ±14.5 V output, >92% efficiency, Auto-PID, zero EMI
ATE1-127 (>8 A), multi-stage, high-Vmax arrays	TEC24V10A-D	10 A	24 V input, ±23.5 V output, >92% efficiency, Auto-PID, zero EMI, no ext. heatsink
ATE1-127-15AS, ATE1-127-30AS, multi-module	TEC18V15A-D	15 A	18 V input, ±14.5 V output, highest current, >92% eff., Auto-PID, zero EMI

Table 16: Recommended ATI TEC controller for each module series. ATI precision TEC controllers provide current-regulated, low-ripple drive.

Browse the complete TEC module catalog and pricing: [ATI TEC Module Selection Guide & Price List].

PART III — SYSTEM DESIGN

Building the Complete Thermal Loop

For high-power applications (>100 W TEC load) requiring 24 V supply rails — common in industrial, telecom, and AI server thermal management — ATI offers the TEC24V10A series (24 V input, ±10 A, ±23.5 V output) and TEC18V15A series (18

V input, ±15 A, ±14.5 V output). Both achieve >92% efficiency with Auto-PID compensation, zero EMI, and ±0.001 °C temperature stability — no external heat sink required for most operating conditions. These controllers pair naturally with the ATE1-127-12AS, ATE1-127-15AS, and multi-module configurations used in high-power cooling and active heat spreading (see www.analogtechnologies.com/TEC_Controller_TEC28V15A_series.html).

8. The ATI Ecosystem — Controllers, Thermistors, Heat Sinks

A TEC module is only one piece of the thermal-management puzzle. A complete, reliable temperature-control system requires a precision controller, a well-placed thermistor, and a properly sized heat sink — all designed to work together. Before we move to the worked examples in Section 9, here is the ecosystem you will use to build them.

Important: Do not drive a TEC from an uncontrolled voltage source. TEC resistance, Seebeck voltage, and hot-side temperature interact; direct voltage drive can cause excessive current, thermal runaway, poor stability, and shortened module life. Always use a current-regulated TEC controller with temperature feedback.

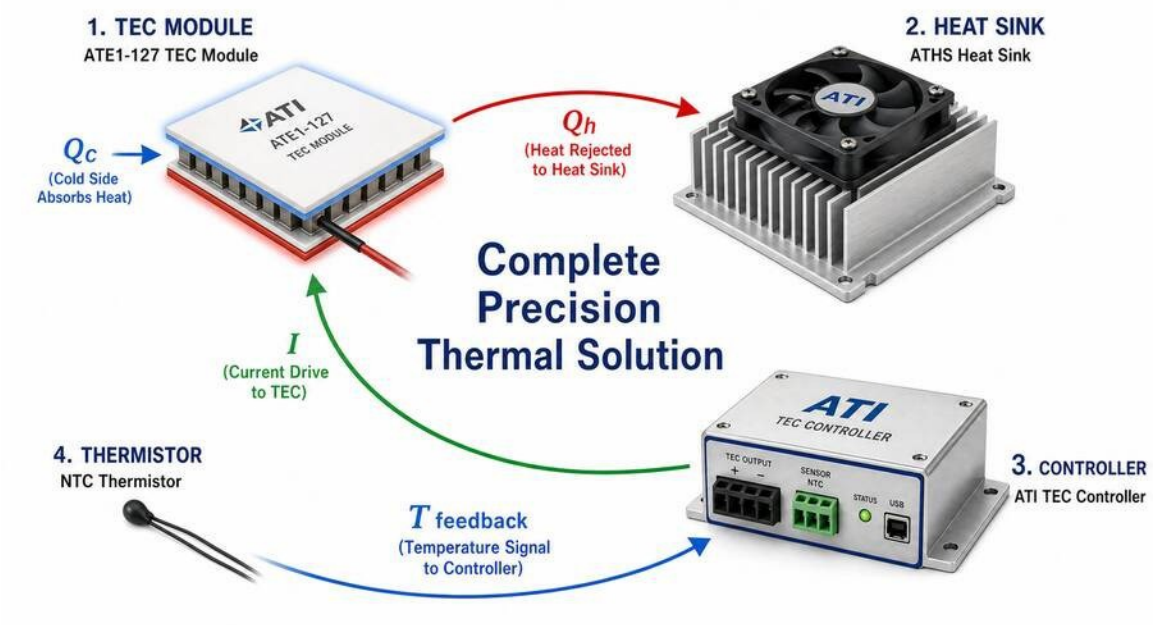

Figure 18: *The complete ATI TEC ecosystem. Four components — TEC module, heat sink, controller, and NTC thermistor — form a closed-loop precision thermal*

system. The controller drives current I to the TEC based on the thermistor's temperature feedback; heat flows Qc → Qh from the device into the heat sink.

8.1 TEC Controllers

Browse the full TEC controller product line (www.analogtechnologies.com/tec-controller) for current specifications, datasheets, and pricing.

Controller	I_{max}	Vin	Temperature stability	Recommended ATE1-127 range
TEC14M5V3R5AS	3.5 A	5 V	±0.002 °C	Up to 3 A — precision laser, DFB
TEC14M5V5AS	5.0 A	5 V	±0.005 °C	3–5 A — small laser modules, CCD
TEC14M12V8AS	8.0 A	12 V	±0.005 °C	5–8 A — optical modules, IR detectors
ATFC109D	10 A	12 V	±0.01 °C	8–10 A — analytical instruments
TEC18V15A	15 A	18 V	±0.001 °C	10–15 A — cold plates, PCR cyclers
TEC24V10A-D	10 A	24 V	±0.001 °C	8–10 A — 24 V rail, industrial, telecom, AI server cooling
Custom ATFC30+	30 A	24 V	±0.05 °C	15–30 A — liquid chillers

8.2 NTC Thermistors

Critical rule: Use 10 kΩ NTC thermistors (β = 3,977 K, ±1% interchangeability) for temperature feedback. ATI offers matched thermistors with ±0.1 °C interchangeability (no recalibration on replacement), fast thermal response (small bead), long-term stability (< 0.02 °C drift/year), and −40 to +125 °C range. Mount on the cold plate, NOT on the TEC ceramic; within 5 mm of the thermal load; with thermal paste between thermistor and cold plate; and electrically insulated from the cold plate if it is metallic. See the ATI NTC thermistor datasheet for complete specifications. For the complete ATI thermistor portfolio, see the NTC Thermistor Selection Guide

8.3 Heat Sinks — ATHS Series

The ATHS series features flat, lapped mounting surfaces (uniform TIM thickness, minimal R_{TIM}), optimized fin geometry (maximum surface area per volume), pre-drilled mounting holes aligned to standard TEC footprints, and integrated-fan variants with matched airflow. For projects requiring custom thermal solutions (compact liquid cold plates, custom extrusions, full assemblies with fans and ducting), ATI provides design and manufacturing services. View the thermal system components catalog including heat sinks, fans, and thermal pads. Browse the full ATHS heat sink catalog at .

8.4 System Integration Support

ATI does not just sell components — we help engineers design complete thermal-management systems: custom heat-sink design and manufacturing, thermal simulation and analysis, controller selection and configuration, system-level testing and validation, and production support. Contact: sales@analogtechnologies.com · +1 408-748-9100 · www.analogtechnologies.com.

Quick answer: *A complete TEC thermal system needs four matched components — module, controller, thermistor, heat sink — and ATI is one of the few suppliers that designs and manufactures all four to work together as a single ecosystem.*

9. Three Complete Worked Examples

Three start-to-finish designs spanning three different decision boundaries. Every temperature, heat flow, and electrical parameter is internally consistent and uses the equations and curves of Section 5. Follow these examples step by step and adapt to your own application.

9.1 Example A — Laser-Diode Wavelength Stabilization (Compact, Precision)

Requirement: stabilize a single-emitter Fabry-Pérot laser diode on a copper submount at Tc = 20 °C with Qc = 9.5 W of waste heat dissipation, T_{amb} = 25 °C, lab humidity 40–60% RH, target stability ±0.01 °C.

Step 1 — module selection. Applying $Q_{max} \geq 2\times$ Qc gives 19 W minimum; for a laser application where stability and life matter, target 4×: $Q_{max} \geq 38$ W. The ATE1-127-5AS (Q_{max} = 43 W, I_{max} = 5 A, 30×30 mm sealed) gives 4.5× margin, fits in a butterfly-package footprint, and the sealed body protects against condensation since Tc < T_{amb}.

Step 2 — assume the hot-side network. R_{TIM} = 0.15 °C/W (0.1 mm thermal grease each interface), R_{hs} = 0.22 °C/W (80 mm forced-air heat sink).

Step 3 — iterate operating point using the Section 5 equations. The current required to deliver Qc = 9.5 W at the modest ΔT depends on Th, which depends on Qh = Qc + Pin, which depends on the operating point. Using the ATE1-127-5AS parameters (α = 0.0513 V/K, R = 2.38 Ω, K = 0.44 W/K) and solving self-consistently (3 iterations converge): I = 1.00 A, V = α·ΔT + I·R = 0.0513×9.6 + 1.00×2.38 = 2.87 V, Pin = V·I = 2.87 W, Qh = 9.5 + 2.87 = 12.37 W.

Parameter	Symbol	Value	Notes
Operating current	I	1.00 A	I/Imax = 0.20 — Goldilocks zone
TEC terminal voltage	V	2.87 V	α·ΔT + I·R = 0.0513·9.6 + 1.00·2.38
Electrical input power	PTEC	2.87 W	V·I
Cooling power	Qc	9.5 W	Application requirement
Heat rejected	Qh	12.37 W	Qc + Pin
Hot-side temperature	Th	29.6 °C	Tamb + Qh·(RTIM + Rhs) = 25 + 12.37·0.37
Temperature difference	ΔT	9.6 °C	Th − Tc
Coefficient of	COP	3.31	Qc / Pin

Parameter	Symbol	Value	Notes
performance			

Self-consistency check: Th = 25.0 + 12.37 × 0.37 = 29.6 °C ✓. The system sits at the low edge of the Goldilocks zone (I/Imax = 0.20) with COP = 3.31 — excellent for a TEC system. The module is loaded at roughly 22% of Qmax; lifetime under steady-state operation will exceed 200,000 hours.

Step 4 — heat-sink verification. Rhs,max = (50 − 25) / 12.3 − 0.15 = 1.88 °C/W. The chosen 0.22 °C/W heat sink provides ≈8.6× safety margin — plenty of room for dust, fan aging, and elevated summer ambients.

Step 5 — controller selection. ATI TEC14M5V3R5AS (3.5 A, 5 V input, ±0.002 °C stability, linear drive, auto-PID compensation). Output ripple below 0.1% — exactly what a single-mode laser diode needs for ±0.001 nm wavelength stability. Product page | datasheet

Bill of materials: ATE1-127-5AS module + TEC14M5V3R5AS controller + ATI 10 kΩ NTC thermistor (β = 3977 K, mounted on the copper submount within 5 mm of the diode) + 80 mm forced-air heat sink with R_{hs} = 0.22 °C/W + standard silicone thermal grease, 50–100 µm per interface. Order online at shop.analogtechnologies.com.
→ Module: ATE1-127-5AS | Controller: TEC14M5V3R5AS | Thermistor: ATI 10 kΩ NTC

Controller current headroom: The selected operating current of 1.0 A is well below the TEC14M5V3R5AS controller's ±3.5 A capability, providing >3× headroom for transient response and ensuring the controller operates in its most linear, lowest-noise region.

9.2 Example B — Cooled CCD/CMOS Imaging Sensor (Deep ΔT)

Requirement: cool a 24×36 mm full-frame CMOS imager to Tc = −20 °C to suppress dark current for 600-second astrophotography exposures. Sensor dissipation Qc = 4.5 W (bias plus front-end electronics). T_{amb} = 22 °C. Required ΔT = 22 − (−20) = 42 °C — a substantial cold-side excursion.

Step 1 — module selection. ΔT = 42 °C is large; apply the 4× rule: $Q_{max} \geq 18$ W. But the higher ΔT also reduces effective cooling capacity (Fourier back-conduction grows). From Curve 1 in 5.4, at $I/I_{max} = 0.45$ and $\Delta T/\Delta T_{max} = 0.63$ (42/66), $Qc/Q_{max} \approx 0.07$ — a module needs roughly 70 W of Q_{max} to deliver 4.5 W. Choose the ATE1-127-8AS (Q_{max} = 68.9 W, I_{max} = 8 A, 40×40 mm sealed). The sealed body is mandatory — Tc = −20 °C is far below any realistic dew point.

Step 2 — set up the hot-side network. Use a liquid cold plate to keep Th low (lower Th means easier ΔT). R_{TIM} = 0.10 °C/W (premium thermal pad on each side), R_{hs} = 0.10 °C/W (compact liquid cold plate with chiller loop at 18 °C effective ambient).

Step 3 — self-consistent operating point (4 iterations):

Parameter	Symbol	Value	Notes
Operating current	I	3.55 A	I/Imax = 0.44 — above the Goldilocks zone (0.20–0.35); chosen to reach the required 44 °C span
TEC terminal voltage	V	7.59 V	α·ΔT + I·R = 0.0513·44.1 + 3.4·1.50 (bridge values)
Electrical input power	PTEC	26.9 W	V·I
Cooling power	Qc	4.5 W	Sensor + electronics dissipation
Heat rejected	Qh	31.4 W	Qc + Pin
Hot-side temperature	Th	24.1 °C	18 + 30.3·(0.10 + 0.10)
Temperature difference	ΔT	44.1 °C	Th − Tc
Coefficient of performance	COP	0.17	Low — expected for large ΔT

Self-consistency: Th = 18 + 31.4 × 0.20 = 24.3 °C ✓. The low COP (0.17, consistent with Curve 3 in 5.4 at $\Delta T/\Delta T_{max}$ = 0.67) is the inevitable price of the 44 °C span — the ATE1-127-8AS spends most of its energy fighting Fourier back-conduction. To improve COP, the only options are reduce ΔT (warmer Tc target), reduce Th (better hot-side cooling), or accept the power cost. We accept it: 26 W of input power for a 4.5 W deep-cooled science-grade sensor is cheap.

ATE1-127-8AS. Note: The low COP (0.17) is expected and acceptable when large ΔT is the primary design requirement. Deep cooling inherently requires more electrical input per watt of heat pumped.

Controller selection: ATI TEC14M12V8AS (8 A, 12 V input, linear drive). Provides margin over the 3.55 A operating current; 12 V rail supports the 7.6 V TEC voltage with overhead for transients. (TEC controllers) (view TEC14M series)

Lesson: at large ΔT, COP collapses but the application still works. The right question is not “is COP high?” but “is the input power tolerable?” For a benchtop cooled-camera application, 26 W is a non-issue. For a battery-powered field instrument, it might force a different architecture (larger sensor with higher Qc per pixel, less aggressive Tc target, or multi-stage TEC).

9.3 Example C — AI Accelerator Hotspot Cooling (High Power Density)

This example operates in the active-heat-spreading regime introduced in §5.3.4. The TEC's 'cold' side (Tc) is physically warmer than its 'hot' side (Th), so ΔT = Th − Tc is negative. The TEC pumps heat 'downhill' — assisting natural conduction rather than opposing it. COP can exceed 10 because the Peltier effect supplements the thermal gradient.

Requirement: a GPU/TPU silicon die has a localized hotspot near the matrix-multiply unit dissipating 40 W into a 12×12 mm area. The bulk die is held at 65 °C by a high-performance liquid cold plate; the hotspot reaches 95 °C and the chip throttles, costing 15% of inference throughput. Goal: knock the hotspot temperature down to 75 °C so the silicon never throttles. Effective T_{amb} (cold-plate water) = 65 °C; $T_{h,max}$ for the TEC = 90 °C (well within the H-series rating).

Step 1 — module selection. Qc = 40 W localized; ΔT requirement = 95 − 75 = 20 °C. Need $Q_{max} \geq 3 \times 40 = 120$ W to keep current low and lifetime high. The hotspot is small (≈144 mm²), so the module must match — a 40×40 mm footprint at the bottom of a custom heat-spreader works. The ATE1-127 high-temperature variant (ATE1-127-15ASH) (Q_{max} = 126 W, I_{max} = 15 A, 40×40 mm, sealed, H-series for the warm chip environment) is the natural choice.

Step 2 — hot-side network. The TEC sits between the silicon and the liquid cold plate. R_{TIM} = 0.08 °C/W (thin TIM on each side, augmented by mounting pressure). R_{hs} is the cold-plate-to-water resistance ≈ 0.10 °C/W for the matched cold plate. Effective T_{amb} is the water temperature = 65 °C.

Step 3 — self-consistent operating point:

Parameter	Symbol	Value	Notes
Operating current	I	2.0 A	I/I_{max} = 0.13 — deep in efficiency zone
TEC terminal voltage	V	1.4 V	α·ΔT + I·R (low V due to negative ΔT)
Electrical input power	PTEC	2.8 W	V·I — remarkably low
Cooling power	Qc	40 W	Hotspot dissipation
Heat rejected	Qh	42.8 W	Qc + Pin
Hot-side temperature	Th	72.7 °C	65 + 42.8·(0.08 + 0.10)
Cold-side temperature	Tc	75 °C	Achieves the hotspot target
Temperature difference	ΔT	−2.3 °C	Negative! Tc > Th — active heat spreading
Coefficient of performance	COP	14.4	Extremely high — TEC assists natural flow

Self-consistency: Th = 65 + 42.8 × 0.18 = 72.7 °C. Since Tc = 75 °C > Th = 72.7 °C, the temperature difference is negative (ΔT = −2.3 °C). This means the TEC is pumping heat in the natural direction — from the hotter die to the cooler cold plate — acting as an "active heat spreader." The Peltier effect supplements natural conduction, yielding an extraordinary COP of 14.4. Only 2.8 W of electrical input moves 40 W of hotspot heat. This is the sweet spot for embedded TEC cooling: small or negative ΔT with high Qc.

Controller selection: ATI TEC14M12V8AS or a custom ATFC variant matched to the chip's thermal dynamics. The TEC must respond to compute-load transients on a 0.1–1 s time scale — the controller's bandwidth must exceed the cold-plate thermal time constant by 5×–10×. ATI applications engineering supports custom controller tuning for AI thermal-management integration. (product page)

Lesson: hotspot cooling is a low-ΔT (or even negative-ΔT) job — exactly where TECs shine brightest. When the TEC assists natural heat flow rather than fighting it, COP can exceed 10. The total TEC overhead is just 2.8 W — negligible compared to the 700 W GPU power budget. This "active heat spreading" paradigm is why TECs are gaining traction in AI accelerator thermal management.

Physical mounting for negative-ΔT hotspot cooling: In this configuration the TEC cold side faces the hot silicon die (Tc = 75 °C) and the hot side faces the liquid cold plate (Th = 72.7 °C). This is thermally inverted compared to conventional TEC cooling. Key mounting considerations: (1) Use a compliant TIM (phase-change or indium foil, 20–50 µm) between die and TEC cold face to accommodate CTE mismatch between silicon (2.6 ppm/°C) and alumina ceramic (7 ppm/°C). (2) Apply uniform clamping pressure (10–30 psi) across the TEC footprint — uneven pressure creates thermal hotspots and accelerates pellet fatigue. (3) The liquid cold plate must have thermal resistance < 0.15 °C/W to keep Th below the die temperature; use microchannel or jet-impingement designs for high-density applications. (4) Seal the TEC perimeter with RTV silicone to prevent condensation ingress during power-off transients when the cold plate may temporarily drop below dew point. (5) Route thermistor feedback from the die surface (not the TEC ceramic) for accurate hotspot temperature control.

Quick answer: Three worked examples — laser (Qc = 9.5 W, ΔT = 9.6 °C, COP = 3.31), cooled imager (Qc = 4.5 W, ΔT = 44 °C, COP = 0.18), and AI hotspot (Qc = 40 W, ΔT = −2.3 °C, COP = 14.4) — demonstrate that TECs excel across the entire spectrum: from precision temperature control to active heat spreading.

PART IV — BUILD AND OPERATE

Assembly, Pitfalls, and Long-Term Reliability

Interpretation note: The Qc = 40 W is the total heat crossing the TEC's cold face. A passive thermal path from die to cold plate would already conduct a substantial fraction of this heat. The TEC input power (2.8 W) is the incremental power needed to actively reduce the die temperature from its passive-conduction equilibrium (~85–90 °C) to the regulated 75 °C target. The high COP reflects the efficiency of active heat spreading at near-zero ΔT, but should not be interpreted as the TEC pumping 40 W against zero thermal resistance.

10. Mounting, Wiring, and Assembly Best Practices

Quick answer: Use thin, uniform thermal grease (50-100 um), mount hot-side down, never exceed 0.2–0.4 N·m (for M3 screws) torque, and always seal against condensation when Tc is below dew point.

A perfectly selected TEC with an ideal controller will still fail if assembled incorrectly. This chapter covers the practical details that separate a reliable production system from a frustrating prototype.

10.1 Thermal Interface Material (TIM)

Apply a thin, uniform layer of thermal grease (25–100 µm (25 ± 13 µm with fine-screen roller; 50–100 µm hand-applied)) to BOTH sides of the TEC — between the TEC hot side and the heat sink, and between the TEC cold side and the device cold plate.

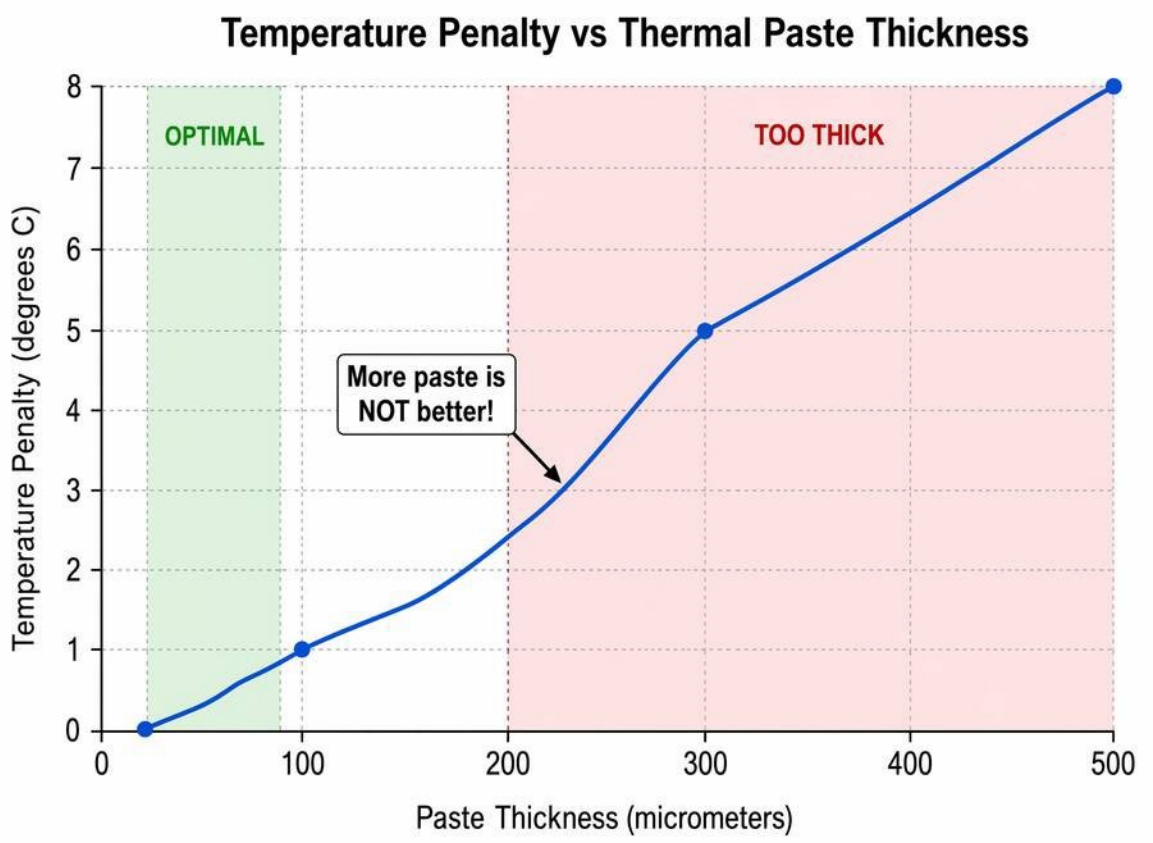

Figure 19: *Effect of thermal-paste thickness on temperature penalty. Below 100 µm, the penalty is negligible (filling microscopic surface voids). Above 200 µm, the paste itself becomes a thermal insulator — more paste is NOT better.*

Paste thickness	R_{TIM} per interface	Temperature penalty at 12 W
50 µm (ideal)	0.05 °C/W	0.6 °C
100 µm (acceptable)	0.10 °C/W	1.2 °C
200 µm (too much)	0.20 °C/W	2.4 °C
500 µm (way too much)	0.50 °C/W	6.0 °C

Rule: apply a small amount and spread with a flat-edge spatula or a stencil. The goal is to fill microscopic surface voids — not to create a thick insulating layer. If paste squeezes out the sides when you clamp, you used too much.

10.2 Mounting Stack and Assembly Order

- Heat sink (hot-side thermal mass) For pre-assembled solutions, see the TEC Assembly series.
- TIM layer (50–100 µm thermal grease)
- TEC module (hot side DOWN — wires exit from the hot side)
- TIM layer (50–100 µm thermal grease)
- Cold plate / device (your thermal load)

Use four screws with spring washers for uniform compression. Torque to 0.2–0.4 N·m for M3 screws. Target compression 1.0–2.0 MPa (150–300 PSI).

Critical: The label/printing is on the COLD side of ATI modules. When mounting, the cold side (label side) faces UP toward your device. The hot side (wire side) faces DOWN toward the heat sink. Reversing this heats your device instead of cooling it.

10.3 Step-by-Step Assembly Procedure

The quality of a TEC assembly is determined not by the module alone, but by the mechanical and thermal integrity of every interface in the stack. A poorly assembled system can lose 20–40% of its theoretical cooling capacity to parasitic thermal resistance — the thermal equivalent of building a high-performance engine and connecting it to the wheels with a rubber band. The following procedure, refined over decades of field experience, ensures repeatable, high-performance assemblies.

Surface Preparation. Both the heat-sink base and cold-plate mating surfaces must be ground or lapped flat to within ±0.025 mm across the module footprint, with a maximum total indicated reading (TIR) of 0.076 mm. Remove all burrs, chips, and foreign matter from the mounting area. For multi-module arrays sharing a common base plate, the TEC thickness variation between modules must not exceed ±0.025 mm — specify tolerance-lapped modules when ordering.

Thermal Interface Application. Apply a thin, continuous film of thermal grease to the module hot-side surface and to the corresponding area on the heat exchanger. Target grease thickness is 25 ± 13 µm — just enough to fill microscopic surface voids without creating a resistive layer. A printer's ink roller with a fine screen provides excellent thickness control for production environments.

Module Placement. Place the TEC module on the heat exchanger with the hot side facing down (wires exit from the hot side). Gently oscillate the module back and forth while applying uniform downward pressure. Continue the oscillation until you observe thermal compound efflux around the module edges and feel mechanical resistance — this confirms intimate surface contact with minimal trapped air.

Cold-Plate Mating. Repeat the grease application on the module cold side and cold-plate surface. Position the cold plate on the module and repeat the oscillation technique. Maintain uniform pressure throughout — keep the module centered between the mounting screws to prevent uneven compression that would crack the ceramic substrate.

Fastening and Compression. Before final bolting, preload the assembly in compression using a light clamp or calibrated weights aligned with the module center. For multi-module assemblies, use three screws along the module centerline and torque the middle screw first. Apply torque in small increments, alternating between screws, using a torque-limiting screwdriver. The recommended compression is 10–21 kg/cm² (150–300 PSI) of module surface area.

The torque per screw is: $T = (C \times D \times P \times A) / N$, where T is torque (N·m), C is the torque coefficient (0.20 dry, 0.15 lubricated), D is nominal screw diameter (m), P is target pressure (Pa), A is module surface area (m^2), and N is the number of screws. Use stainless-steel screws with fiber-insulating shoulder washers and steel spring washers (Belleville or split-lock type). Check torque after one hour and retighten if necessary — thermal grease settles under initial load.

Critical caution. Excessive torque on thin substrates causes bowing, which creates an air gap at the module center and dramatically increases thermal

resistance. Reduce torque if either mating surface is thinner than 3.2 mm (copper) or 6.4 mm (aluminum). When in doubt, use a pressure-indicating film (such as Fujifilm Prescale) to verify uniform contact pressure across the module footprint.

Never apply shear force to the TEC during assembly. Bi_2Te_3 pellets are brittle ceramics — lateral force cracks them. Use alignment pins or a fixture, then apply only compressive (downward) force.

10.4 Wiring and Soldering

TEC lead wires must be soldered carefully to avoid heat damage to internal solder joints. Standard series: iron tip 280 °C, ≤ 3 s per joint, ≥ 10 mm from module body, SAC305 solder. H-series: iron tip 320 °C, ≤ 5 s per joint. If you must solder closer than 10 mm, clamp a heat sink (alligator clip or copper strip) on the wire between the iron and the TEC module.

10.5 Polarity and Wiring Convention

- Red wire = positive (+); Black wire = negative (−).
- Current red-to-black (conventional direction) cools the labeled (cold) side.
- Connect red to TEC+ on the controller, black to TEC−.
- If the system heats instead of cools, swap the wires — the most likely cause is reversed polarity.

10.6 Dew Point and Condensation Management

When the cold side operates below the local dew point, water condenses on it — corroding Bi_2Te_3 elements, shorting traces, contaminating optical surfaces, and eventually causing open-circuit failure. Use sealed (S) variants when Tc < dew point. At 25 °C and 60% RH the dew point is about 16.7 °C. For critical applications add a dry-gas (N_2 or dry air) purge or a desiccant pack in a sealed enclosure.

10.7 Insulation, Sealing, and Spacer-Block Design

Once the TEC modules are assembled between heat exchangers, the space surrounding the modules must be insulated and sealed. The TEC element matrix is an open DC circuit operating under a temperature gradient — uncontrolled air flow through this region causes condensation on the cold elements, accelerates corrosion of the Bi_2Te_3 semiconductor, and degrades performance over time.

Why insulate? A standard single-stage TEC is approximately 5 mm thick. Without insulation, the short thermal path between hot and cold exchangers allows

parasitic heat conduction through the surrounding air gap, reducing net cooling capacity by 5–15% depending on geometry and ΔT. At high ΔT (approaching ΔT_{max}), this parasitic loss becomes the dominant limiter of system performance.

Recommended insulation method. Insert die-cut closed-cell polyurethane foam around the module cavity. Seal the perimeter with RTV silicone for moisture protection, or epoxy for applications requiring mechanical integrity. The seal serves three purposes simultaneously: thermal insulation, moisture barrier, and mechanical strain relief for the lead wires. Whatever sealant is used, ensure it does not outgas corrosive volatiles near the TEC elements.

Spacer-block technique. For maximum performance in high-ΔT applications, use thermally insulating spacer blocks to increase the physical separation between hot and cold exchangers beyond the TEC thickness alone. Place spacer blocks on the cold side of the assembly — the lower heat-flux density on the cold side means the added thermal path has minimal impact on system COP, while the increased insulation distance dramatically reduces parasitic conduction from the hot side. Think of it as adding a longer hallway between a furnace room and a freezer — the extra distance costs almost nothing in cooling effort but blocks a great deal of unwanted heat leakage.

10.8 Current Ripple

Ripple from PWM controllers or switching supplies adds extra Joule heating (I^2R, where I includes the ripple) without contributing to Peltier cooling (which responds only to the DC average). Net cooling capacity drops and temperature stability degrades.

Application	Maximum allowable ripple (peak-to-peak)
General cooling	< 10% of DC current
Precision temperature control	< 5% of DC current
Laser diode wavelength stability	< 2% of DC current
Ultra-precision (millikelvin)	< 1% of DC current

ATI's linear TEC controllers deliver ripple below 0.1% — orders of magnitude better than PWM-based alternatives. Where an upstream switching supply is unavoidable, add an LC filter between the supply and the controller input.

Current ripple in TEC systems originates from three sources: (1) the TEC controller switching topology, (2) the upstream power supply, and (3) coupled electromagnetic noise from adjacent circuits. For precision applications (laser

diodes, single-photon detectors, optical coherence tomography), ripple must be suppressed below 0.1% of the DC operating current. ATI linear-drive TEC controllers achieve this inherently — no output LC filter is required. For PWM-based controllers (not recommended for precision work), size the output LC filter with $L = V_{ripple} / (2\pi \cdot f_{sw} \cdot I_{ripple})$ and $C = I_{ripple} / (2\pi \cdot f_{sw} \cdot V_{ripple})$, targeting $f_{sw} > 100$ kHz to push harmonics above the thermal time constant. All ATI TEC controllers feature full metal shielding (Faraday cage construction), achieving conducted EMI below CISPR 32 Class B limits without external filtering. For applications requiring zero EMI (MRI environments, sensitive RF receivers), linear drive is mandatory — see the TECA1 series controllers.

10.9 EMI/EMC Considerations for TEC Systems

TEC modules themselves produce no electromagnetic interference because they are purely resistive DC loads. However, the TEC controller's switching frequency (typically 100–500 kHz for PWM types) can radiate if the wiring between controller and module is not properly managed. Best practices: (1) keep TEC power leads short and twisted or use shielded cable, (2) place a ceramic bypass capacitor (100 nF, X7R) directly at the TEC module terminals, (3) use a fully shielded controller enclosure — all ATI TEC controllers are factory-shielded to meet CISPR 32 Class B conducted and radiated limits, and (4) route TEC power leads away from sensitive analog signal paths, especially thermistor sense lines.

10.10 NTC Thermistor Placement

Mount the NTC thermistor on the cold plate (NOT on the TEC ceramic surface) and as close to the thermal load as possible (≤ 5 mm). This ensures the controller regulates the temperature that matters — the device's, not the TEC surface's. Mounting on the TEC ceramic puts the R_{TIM} resistance between the measurement point and the actual load, producing an uncontrolled offset that varies with heat load and paste thickness.

Quick answer: *Apply thin TIM (25–100 µm) per interface, compression only (never shear), label-side-up toward the load, ripple < 5% (< 2% for lasers), thermistor on the cold plate within 5 mm of the device.*

10.8 Dynamic Behavior and Transient Design

A TEC system is not instantaneous. The thermal time constant $\tau = C_{thermal} / K_{total}$ typically ranges from 10 to 60 seconds depending on the thermal mass of the cold-side load. Understanding transient behavior is essential for applications requiring fast temperature switching or tight settling-time specifications.

Key design parameters for transient performance:

Thermal time constant (τ): Determined by the total thermal capacitance (mass × specific heat of the cold-side assembly) divided by the effective thermal conductance. Smaller loads settle faster. A bare TEC ceramic reaches 90% of its final ΔT in approximately 30 seconds; a copper block with an optical component may take 2–5 minutes.

Overshoot and settling: Aggressive PID tuning (high proportional gain, short integral time) reduces settling time but risks overshoot. For precision applications requiring ±0.01 °C stability, use conservative tuning with derivative action to damp oscillations. ATI controllers with auto-PID compensation handle this automatically.

Controller bandwidth: The controller must respond faster than the thermal disturbance frequency. For most TEC systems, a control-loop bandwidth of 0.1–1 Hz is sufficient. Higher bandwidth is needed only for fast-switching applications (e.g., PCR thermal cycling at 2–5 °C/s ramp rates).

Feedforward compensation: When the heat load varies predictably (e.g., a laser diode turning on/off), adding a feedforward term to the controller output reduces the transient excursion by pre-loading the TEC before the disturbance arrives. This technique can reduce settling time by 50–70% compared to feedback-only control.

Practical guideline: For settling time < 60 s, minimize cold-side thermal mass (thin cold plate, direct die attach). For settling time < 10 s, consider reducing module size (fewer pellets = lower thermal capacitance) and using feedforward. For sub-second response, TEC alone is insufficient — combine with thermoelectric pre-conditioning and fast optical/electronic compensation.

11. Top 10 Ways to Ruin Your TEC — Common Pitfalls

We have seen every TEC design mistake across thousands of customer applications. Here are the top ten, with the physics of why each hurts and the specific fix.

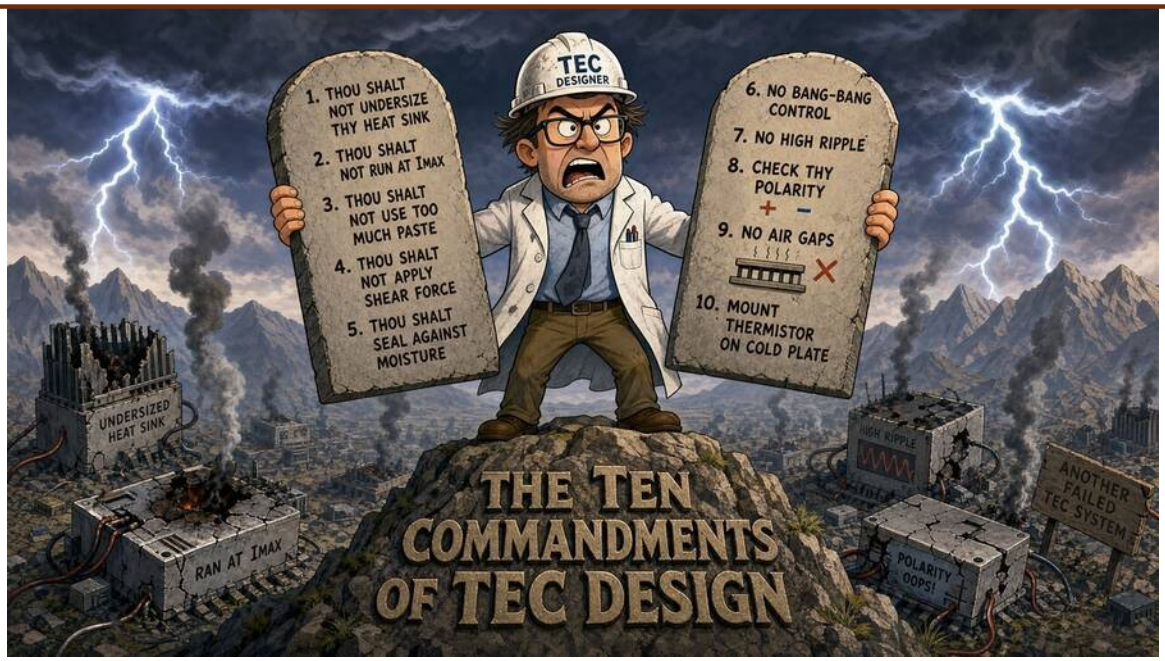

Figure 20: The Ten Commandments of TEC Design. The stone tablets list the ten most critical TEC design rules; violating any one risks system failure: undersized heat sinks, running at Imax, paste overload, polarity reversals, and high ripple.

#	Mistake	Why it hurts	The fix
1	Undersized heat sink	Th rises uncontrollably → thermal runaway	Size for Qh = Qc + Pin; add 30% margin
2	Running at I_{max}	COP < 0.5, massive waste heat, short life	I = 0.20–0.35·I_{max}; pick a larger module if needed
3	Too much thermal paste	Each interface adds 2–6 °C of penalty	Thin uniform layer 50–150 µm; spatula or stencil
4	Shear force on assembly	Cracks Bi_2Te_3 pellets → open circuit	Compression only; alignment pins/fixture
5	No moisture protection	Corrosion → open circuit	Sealed (S) variant when

#	Mistake	Why it hurts	The fix
		over months	Tc < dew point
6	On/off (bang-bang) control	±2 °C oscillation; thermal cycling fatigue	PID controller (ATI family) with auto-tune
7	High current ripple (>10%)	Extra I^2R; net Qc drops, laser jitter rises	Linear controller, < 5% ripple; LC filter if needed
8	Reversed polarity	TEC heats your device instead of cooling it	Red = +, Black = −; label side = cold
9	Air gaps in the stack	Air $R_th \approx 40\times$ worse than paste	Spring-loaded screws; flat lapped surfaces
10	Thermistor on TEC ceramic	Regulates TEC surface, not the load	Mount on cold plate within 5 mm of load

Quick answer: *The five most common TEC field failures — undersized heat sink, running at Imax, paste overload, shear-cracked pellets, and unprotected cold sides below the dew point — account for over 80% of every TEC system that ever stopped working in the field.*

12. Reliability, Lifetime, and Qualification

TEC modules are inherently reliable — no moving parts, no wear-out mechanisms under steady-state operation. Understanding the failure mechanisms that DO exist allows engineers to design systems that achieve 20+ years of continuous service.

12.1 Why TECs Fail

The primary failure mechanism is thermo-mechanical fatigue caused by differential thermal expansion between the ceramic substrates, solder joints, and Bi_2Te_3 pellets during thermal cycling. Each cycle creates microscopic stress at the solder interfaces; over thousands of cycles, fatigue cracks nucleate and propagate

until a solder joint opens. Secondary mechanisms: moisture-induced corrosion through unsealed edges, electromigration at extreme current densities, and oxidation of Bi_2Te_3 at elevated temperatures.

12.2 Lifetime Guidelines

Operating condition	Expected lifetime	Notes
Steady state (constant ΔT)	> 200,000 h (> 22 years)	The gold standard — no cycling stress
Moderate cycling (ΔT < 40 °C, < 1/h)	> 100,000 cycles	Typical for precision instruments
Aggressive cycling (ΔT > 60 °C, > 10/h)	10,000–50,000 cycles	PCR, environmental chambers
Sealed (S) in 85 °C / 85% RH	2–5× longer than unsealed	Humidity-accelerated testing

12.3 Design for Long Life

- Minimize thermal cycling amplitude — every degree of ΔT swing stresses the joints.
- Ramp slowly (≤ 2 °C/s) — fast transients multiply internal gradient stress.
- Operate at low I/I_{max} — less Joule heating, lower Th, less stress.
- Use sealed variants — humidity fluctuates even in “dry” rooms.
- Keep Th below 80 °C — high Th accelerates all degradation mechanisms.

12.4 AC-Resistance Health Monitoring

AC resistance at 1 kHz, 25 °C is the best non-destructive indicator of TEC health. Establish a baseline RAC when the module is new, then monitor periodically:

• < 5% deviation from baseline: Normal — no action required.
• 5–10% deviation: Early warning — schedule inspection at next maintenance window.
• 10–20% deviation: Degradation confirmed — plan replacement.
• > 20% deviation: End-of-life — replace immediately.

DC resistance is unreliable for this check because it varies strongly with temperature and contact resistance; always use 1 kHz AC at 25 °C.

12.5 Qualification Standards

The ATE1-127 series modules are RoHS 3 and REACH compliant, qualified to IPC/JEDEC J-STD-020 (MSL 1), tested per 85 °C/85% RH humidity for sealed variants (1,000 h pass), and manufactured under ISO 9001:2015.

Quick answer: *TEC lifetime is dominated by thermal-cycling fatigue; steady-state operation has demonstrated lifetimes exceeding 200,000 hours under controlled conditions, and AC-resistance trending is the best early-warning indicator.*

12.5.1 Functional Performance Testing

Before deploying a TEC in a system, functional testing verifies that the module meets its datasheet specifications. The standard test uses a vacuum temperature-difference tester — a controlled environment that eliminates convective losses and provides repeatable, traceable measurements.

The TEC is placed on a temperature-controlled heat sink with the cold side facing upward, inside a vacuum chamber. A calibrated copper block with an embedded resistive heater serves as the thermal load on the cold side. Two measurements are performed:

ΔT_{max} test: drive the TEC at its rated I_{max} with zero heat load (heater off). The measured temperature difference between hot and cold sides must match the datasheet ΔT_{max} within ±2 °C. Any shortfall indicates degraded thermoelectric material, cracked solder joints, or poor thermal contact in the test fixture. Recall from Section 5.5 that ΔT_{max} depends on Th — ensure the hot side is held at the datasheet reference temperature (typically 27 °C = 300 K).

Q_{max} test: with Th and Tc equalized ($\Delta T = 0$) by adjusting the heater, measure the electrical power delivered to the heater at thermal equilibrium. This power equals Q_{max} — the maximum heat the TEC can absorb at zero temperature lift. Compare against the datasheet value; a deficit exceeding 5% warrants investigation.

12.5.2 Environmental Qualification Test Suite

For applications requiring formal qualification — telecom, aerospace, autonomous vehicles, medical diagnostics — the following test suite validates TEC integrity under accelerated stress conditions. The framework is based on Telcordia GR-468 Core Issue 2, supplemented by application-specific requirements. The universal pass/fail criterion is AC resistance (ACR) measured at 1 kHz, 25 °C: a shift exceeding 5% (early warning) / 10% (investigate) / 20% (end-of-life replacement) from the pre-test baseline indicates internal degradation.

RAC health thresholds: <5% change = normal operation; 5–10% = early warning, schedule inspection; 10–20% = degradation confirmed, plan replacement within 6 months; >20% = end-of-life, replace immediately.

High-Temperature Storage. The TEC is placed unpowered in a storage chamber at 120–150 °C for 1000+ hours. This test reveals solder-joint creep and intermetallic growth under sustained thermal stress — failure modes that would take years to manifest at normal operating temperatures.

Power Cycling (On/Off). The TEC is powered on and off for a set duration per cycle, accumulating a minimum of 5000 cycles. Each on/off transition induces thermo-mechanical stress at the solder joints as the module transitions between ambient and operating temperatures. This test simulates equipment that powers up daily.

Reverse Power Cycling. The TEC is subjected to rapid polarity reversals, alternating between heating and cooling modes with temperature swings of 10–100 °C. This test is particularly relevant for PCR (polymerase chain reaction) thermal cyclers and burn-in test sockets, where modules must survive 200,000+ cycles. ATI's SnSb high-temperature solder construction (H-series) is specifically designed for this regime.

Thermal Shock. The unpowered TEC is transferred between high-temperature and low-temperature chambers (typically +125 °C to −40 °C) with transfer times under 10 seconds. Repeated rapid expansion and contraction stress the ceramic-to-solder interfaces — the most vulnerable point in the TEC construction.

HALT (Highly Accelerated Life Test). The TEC is powered and subjected to progressively increasing thermal and mechanical stress until failure occurs. HALT identifies the module's true operating limits and reveals latent design weaknesses early in the product development cycle — it answers the question "how much margin do we actually have?"

HASS (Highly Accelerated Stress Screening). Similar to HALT but at reduced stress levels, HASS screens production lots for manufacturing defects without destroying good modules. It is a production-line tool, not a design-validation tool.

Compliance. ATI TEC modules comply with RoHS 3, REACH, TSCA, and California Proposition 65. Modules intended for telecom, autonomous-vehicle, or aerospace applications are additionally qualified to Telcordia GR-468 Core Issue 2.

PART V — CONTEXT AND OUTLOOK

Quick answer: TECs excel wherever you need precise, compact, vibration-free temperature control - from stabilizing laser wavelengths to cooling AI accelerator hotspots.

Applications, History, and Where the Field Is Headed

13. Applications — From Lasers to AI

Thermoelectric coolers serve an extraordinary range of applications across virtually every engineering discipline. Here are the categories where TECs are not just the right answer — they are often the only answer.

Application	**Why TEC is the right tool**	**Typical** ATE1-127 + controller
DFB laser wavelength lock (DWDM)	±0.001 nm requires ±0.005 °C — only TEC	ATE1-127-3AS + TEC14M5V3R5AS
Cooled CCD/CMOS imaging	Dark current ~2× per 7 °C; need −20 to −40 °C	ATE1-127-5AS/-8AS + TEC14M12V8AS
PCR thermal cycling	Heat to 95 °C and cool to 55 °C in 40×40 mm	+ TEC12V10A-DATE1-127-10AS
AI accelerator hotspot cooling	Local hotspot lift 20–30 °C without bulk overcool	ATE1-127-15ASH + custom controller
OCXO / atomic frequency reference	Bidirectional stabilization at any setpoint	ATE1-127-4AS + TEC14M5V5AS
LiDAR laser + APD detector	Automotive −40 to +85 °C; orientation-free	ATE1-127-3AH + compact controller
Medical sample / reagent cooling	Quiet, vibration-free, compact	ATE1-127-4AS to -8AS
Quantum photonics / SPAD cooling	Zero vibration, millikelvin precision	ATE1-127-3AS + TEC14M5V3R5AS
Mass spectrometry / analytical	Stable reference cell temperature	ATE1-127-6AS to -10AS

Application	Why TEC is the right tool	Typical ATE1-127 + controller
IR sensor (MWIR/LWIR) cooling	Reduce thermal noise floor	ATE1-127-5AS to -8AS, sealed
Telecom / Fiber Optics	TO-can laser diode cooling in ultra-compact spaces	ATE1-07-3AS + TEC5V4A-D
Small Sensors	DFB lasers and photodetectors requiring precise 6×6 to 12×12 mm footprint	ATE1-17-3AS + TECA1-5V-5V-D
CCD/CMOS Imaging	Scientific cameras requiring 20×20 mm format and ~15 W cooling	ATE1-49-4AS + TEC14M5V5AS
Deep Cooling	High-ΔT applications requiring up to 74.5 °C differential	ATE1-63-3.4AS + TEC14M12V8AS

Quick answer: *Anywhere precision, silence, compactness, sub-ambient capability, or bidirectional control is required, and the cooling load is below ≈200 W, a TEC is almost always the right choice.*

14. A Brief History of Thermoelectrics

The story of thermoelectric cooling spans nearly two centuries — from a curious laboratory observation in 1834 to the precision systems cooling today's most advanced technologies.

Year	Milestone	Significance
1821	Seebeck discovers the Seebeck effect	Voltage from a temperature difference across two dissimilar materials

Year	Milestone	Significance
1834	Peltier discovers the Peltier effect	Current through a junction cools one side and heats the other
1851	Thomson (Kelvin) unifies the thermodynamics	Connects Peltier, Seebeck, and Thomson effects in one framework
1909	Altenkirch derives the figure of merit Z	Shows that good TE materials need high α, low R, low K simultaneously
1954	Goldsmid & Douglas demonstrate Bi_2Te_3	First material with ZT ≈ 1 at room temperature — practical TEC cooling possible
1960s	First commercial TEC modules	Military/aerospace: missile guidance, satellite instruments
1970s	Telecom adoption	Laser diode cooling for fiber-optic systems drives volume production
1980s	Medical and scientific instruments	PCR cycling, detector cooling, reference ovens
1997	Analog Technologies founded	Mission: make precision temperature control accessible
2004	ATI begins TEC module manufacturing	the ATE1-127 series enters continuous production
2010s	Nanostructured materials push ZT > 1.5	Superlattices, quantum dots, nanocomposites

Year	Milestone	Significance
2020s	Thin-film TECs, AI hotspot cooling	Thermoelectric renaissance driven by new applications

14.1 The Goldsmid Breakthrough

Before 1954, no known material had a figure of merit high enough to make TEC cooling practical. The best metals (bismuth, antimony) had ZT < 0.1 — ΔT_{max} of only a few degrees. H. Julian Goldsmid, working at the General Electric Company research laboratory in Wembley, England, recognized that semiconductors — not metals — were the path forward. Semiconductors could have high Seebeck coefficients (carrier concentration is tunable) while maintaining reasonable electrical conductivity. His systematic study of bismuth telluride (Bi_2Te_3) revealed ZT ≈ 1 at room temperature — a tenfold improvement over the best metals. Seventy years later, Bi_2Te_3 remains the dominant material for room-temperature TEC modules.

14.2 ATI's Contribution

Analog Technologies entered the thermoelectric field in 1997 with a clear mission: make precision temperature control accessible, reliable, and affordable. The founders recognized that excellent TEC modules were useless with equally excellent controllers — and that most available controllers were either too noisy (PWM-based), too imprecise (on/off), or too expensive (laboratory instruments). ATI designed controllers from the ground up for TEC applications: patented high-efficiency topologies, auto-PID compensation, fully shielded housings, and linear drive. In 2004, ATI began manufacturing TEC modules in-house, becoming one of the few suppliers offering a fully vertically integrated TEC ecosystem — module, controller, thermistor, and heat sink under one roof — at a time when most competitors specialized in only one or two of those components.

Quick answer: *Modern TEC cooling rests on Peltier**'s 1834 observation, Altenkirch**'s 1909 figure of merit, and Goldsmid's 1954 Bi_2Te_3 breakthrough — and Bi_2Te_3 remains the dominant room-temperature TE material seven decades later.*

15. The Future — Nano-TECs, Advanced Materials, and Beyond

The thermoelectric field is experiencing a renaissance, driven by advances in materials science, manufacturing technology, and an explosion of new applications that demand precision thermal management.

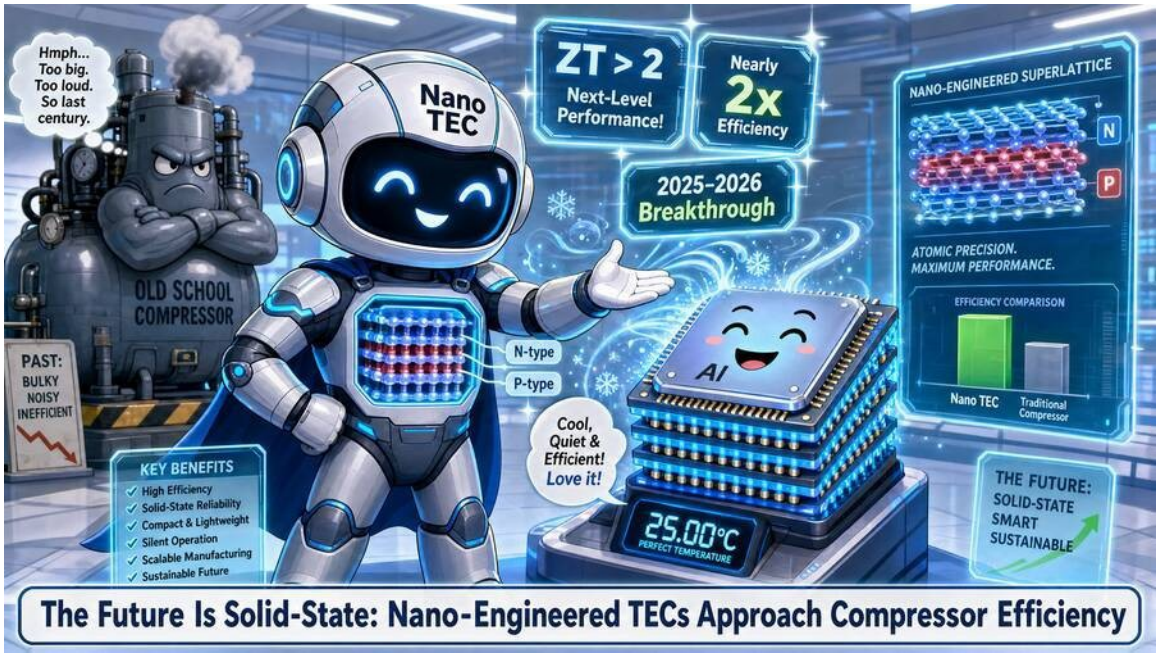

Figure 21: *The future is solid-state. Nano-engineered TEC modules approaching ZT > 2 are positioned to displace bulky compressors in many precision cooling applications — quieter, smaller, with no refrigerants and atomic-precision performance.*

15.1 Micro-TECs and Thin-Film Thermoelectrics

Research-grade miniaturized TEC modules under 5 mm — some smaller than a grain of rice — enable thermal management at the individual chip level. These micro-TECs achieve ΔT > 60 °C in packages that can be flip-chip bonded directly onto semiconductor dies. Thin-film thermoelectrics go further: TE layers deposited directly onto semiconductor wafers using standard fab processes, enabling on-chip cooling without separate modules — promising for 5G RF amplifiers, quantum-computing cryostat stages, and photonic integrated circuits. ATI's miniature TEC controllers are designed specifically for these applications — see the Micro TEC Controller series.

15.2 New Materials Beyond Bi_2Te_3

Material class	ZT (peak)	Temperature range	Promise
Bi_2Te_3 (conventional)	~1.0	−50 to +150 °C	Proven, reliable, cost-effective
Nanostructured Bi_2Te_3	1.2–1.8	−50 to +150 °C	20–80% efficiency improvement
Skutterudites ($CoSb_3$)	1.5–1.7	200–600 °C	Mid-T waste-heat recovery
Half-Heusler alloys	1.0–1.5	300–700 °C	Robust, earth-abundant
SnSe (single crystal)	2.6	500–900 °C	Highest ZT ever measured
Organic / printable	0.1–0.4	0–150 °C	Flexible, low-cost

15.3 Energy Harvesting — TEGs

Running a TEC “in reverse” — applying a temperature difference instead of current — generates electricity via the Seebeck effect. Thermoelectric generators (TEGs) are finding applications in wearable devices powered by body heat, industrial waste-heat recovery, remote sensor nodes powered by geothermal gradients, and automotive exhaust recovery.

15.4 The Conventional TEC — Still the Gold Standard

Despite these exciting developments, the conventional Bi_2Te_3 TEC module remains the proven, reliable, cost-effective solution for room-temperature precision cooling. The ATE1-127 series represents the state of the art in conventional TEC design: decades of proven reliability, fully characterized performance, a complete matched ecosystem, immediate availability in 49 variants, and engineering support from ATI’s experienced thermal-design team. New materials and form factors will expand the thermoelectric universe — but for today’s precision cooling needs, the engineering case is strong: The ATE1-127 series modules + ATI precision controllers = the complete solution.

Quick answer: *Nano-engineered, thin-film, and skutterudite-based TECs are pushing peak ZT past 2 — but for room-temperature precision cooling today, conventional Bi_2Te_3 modules remain the reliable, proven, cost-effective baseline.*

16. Conclusion and Next Steps

This white paper has taken you from “What is a TEC?” through the complete physics, performance characterization, selection, design, assembly, and application of thermoelectric cooling systems. The key takeaways:

- A TEC is a solid-state heat pump — it moves heat from cold to hot using electricity, with no moving parts, no noise, and millikelvin precision.
- Four datasheet parameters define everything. From Qmax, Vmax, Imax, and ΔT_{max} you can derive all module physics and predict performance at any operating point using the Section 5 curves.
- The Goldilocks zone is I/I_{max} = 0.20–0.35 (Section 5.3 + Curve 4 in 5.4) — maximizes COP, minimizes heat-sink load, and extends lifetime.
- The heat sink must handle Qh = Qc + Pin (Section 5.6 + Curve 5 in 5.4) — not just Qc. This is the single most common design mistake.
- ΔT_{max} depends on Th (Section 5.5 + Curve 7) — and the dependence is strong. Always check the actual achievable span at your real hot-side temperature.
- A complete system needs module + controller + thermistor + heat sink, all designed to work together. The ATI ecosystem provides all four.

Your Next Steps

If you need…	Start here
To select a TEC module	Section 7 flowchart + ATE1-127 datasheet
To size your heat sink	Section 5.6 thermal-network equations
To understand the physics deeply	Sections 4 and 5 (Math + Complete Technical Reference)
Performance data for your operating point	Section 5.4 (Normalized Performance Curve Library)
A worked design example	Section 9 (three examples spanning the design space)

If you need…	Start here
Assembly guidance	Section 10 (mounting, wiring, TIM, condensation)
To avoid common mistakes	Section 11 (Top 10 pitfalls)
Product selection	Section 8 (ATI ecosystem) + www.analogtechnologies.com
Application engineering support	sales@analogtechnologies.com · +1 408-748-9100

Browse TEC modules: www.analogtechnologies.com/tec-module
Browse TEC controllers: www.analogtechnologies.com/tec-controller
Browse thermistors: www.analogtechnologies.com/thermistor
Order online: shop.analogtechnologies.com
Request evaluation boards: www.analogtechnologies.com/evaluation-board
Contact our engineering team: sales@analogtechnologies.com

Appendix A: Equations Cheat Sheet

A.1 Fundamental Energy Balance

Equation	Meaning
$Qc = \alpha \cdot Tc \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$	Net cold-side cooling power
$Qh = Qc + Pin = Qc + V \cdot I$	Total hot-side heat rejection
$V = \alpha \cdot \Delta T + I \cdot R$	Module terminal voltage
$Pin = V \cdot I = \alpha \cdot \Delta T \cdot I + I^2 \cdot R$	Electrical input power
$COP = Qc / Pin$	Coefficient of performance

A.2 Datasheet-to-Physics Bridge

Equation	Derives
$\alpha = V_{max} / Th$	Seebeck coefficient (V/K, total module)
$R = (Th - \Delta T_{max}) \cdot V_{max} / (Th \cdot I_{max})$	Electrical resistance (Ω)
$K = (Th - \Delta T_{max}) \cdot V_{max} \cdot I_{max} / (2 \cdot Th \cdot \Delta T_{max})$	Thermal conductance (W/K)
$Z = \alpha^2 / (R \cdot K)$	Figure of merit (K^{-1})

Note: use Th in Kelvin; ΔT_{max} has the same numerical value in °C and K-difference.

A.3 Maximum Temperature Difference

Equation	Meaning
$\Delta T_{max} = ½ \cdot Z \cdot Tc^2$	Master equation (in terms of Tc)
$\Delta T_{max}(Th) = Th + 1/Z - \sqrt{(2 \cdot Th/Z + 1/Z^2)}$	Exact solution in terms of Th
$Iopt\_\Delta T = \alpha \cdot Tc / R$	Current for maximum ΔT
$Iopt,COP = \alpha \cdot \Delta T / [R \cdot (\gamma - 1)]$, $\gamma = \sqrt{(1+Z \cdot \bar{T})}$	Current for maximum COP

A.4 Thermal Network

Equation	Meaning
$Th = T_{amb} + Qh \cdot (R_{TIM} + R_{hs})$	Hot-side temperature
$R_{hs} \leq (T_{h,max} - T_{amb})/Qh - R_{TIM}$	Maximum allowable heat-sink resistance
$\Delta T_{TIM} = Qh \cdot R_{TIM}$ (per interface)	Temperature drop across thermal interface material

A.5 Quick Design Rules

Rule	Guideline
Module sizing	$Q_{max} \geq$ 4–6× Qc (balanced precision)
Operating current	I/I_{max} = 0.20–0.35 for best COP
Heat-sink margin	Add 20–30% to calculated R_{hs} requirement
TIM thickness	50–150 µm per interface
Thermistor placement	On cold plate, ≤ 5 mm from load
Current ripple	< 5% p-p general, < 2% for lasers
Condensation protection	Sealed variant if Tc < dew point
Hot-side temperature	Target Th ≤ 50 °C for long life

Appendix B: Glossary of Terms and Symbols

Symbol / term	Definition	Units
α (alpha)	Seebeck coefficient — voltage per kelvin of temperature	V/K

Symbol / term	Definition	Units
	difference	
Bi_2Te_3	Bismuth telluride — dominant TE material for room-temperature cooling	—
COP	Coefficient of performance — ratio of useful cooling to electrical input power (Qc/PTEC)	—
ΔT	Temperature difference between hot and cold sides (Th − Tc)	°C or K
ΔT_{max}	Maximum temperature difference at zero heat load and optimum current	°C
I	Operating current through the TEC module	A
I_{max}	Maximum rated current (produces ΔT_{max} at Qc = 0)	A
K	Thermal conductance of the TEC module	W/K
NTC	Negative temperature coefficient thermistor — resistance decreases with temperature	—
Peltier effect	Heat absorption/release at a junction when	—

Symbol / term	Definition	Units
	current flows through dissimilar materials	
Pin	Electrical input power to the TEC (V·I)	W
Qc	Cooling power — heat absorbed from the cold side	W
Qh	Heat rejection — total heat delivered to the hot side (Qc + Pin)	W
Q_{max}	Maximum cooling capacity at ΔT = 0 and I = I_{max}	W
R	Electrical resistance of the TEC module	Ω
R_{AC}	AC resistance at 1 kHz — health-monitoring parameter	Ω
R_{hs}	Thermal resistance of the heat sink to ambient	°C/W
R_{TIM}	Thermal resistance of the thermal interface material	°C/W
Seebeck effect	Voltage generated across a material when a temperature difference is applied	—
T_{amb}	Ambient air temperature	°C
Tc	Cold-side temperature	K or °C

Symbol / term	Definition	Units
	(absolute K for equations)	
TEC	Thermoelectric cooler — a solid-state heat pump using the Peltier effect	—
TEG	Thermoelectric generator — generates electricity from a temperature difference	—
Th	Hot-side temperature	K or °C
TIM	Thermal interface material (grease, pad, phase-change)	—
V	Voltage across the TEC module terminals	V
V_{max}	Maximum voltage at I_{max} and ΔT_{max}	V
Z	Thermoelectric figure of merit = $\alpha^2/(R \cdot K)$	K^{-1}
ZT	Dimensionless figure of merit = $Z \times \bar{T}$	—

Frequently Asked Questions (FAQ)

This FAQ is organized into seven clusters so you can jump directly to the topic you need. For deeper treatment of any answer, follow the section references back into the body of this white paper.

CLUSTER A — TEC Basics and Physics

What is a thermoelectric cooler?

A thermoelectric cooler (TEC), also called a Peltier module or Peltier cooler, is a solid-state device that moves heat from one ceramic surface to another when DC current flows through it. It has no

compressor, no refrigerant, no moving parts, and no vibration. A typical module contains 127 N–P Bi_2Te_3 semiconductor couples sandwiched between two alumina (Al_2O_3) ceramic plates. Reversing the current reverses the heat-pumping direction, making a single device capable of both cooling and heating.

How does a TEC module work?

A TEC exploits the Peltier effect: current through N-type and P-type Bi_2Te_3 semiconductor junctions causes electrons to carry thermal energy from the cold junction to the hot junction. Net cooling is the Peltier pumping minus Joule heating and back-conduction: $Qc = \alpha \cdot Tc \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$. The cold side absorbs heat from your device; the hot side rejects that heat plus the electrical input power to the heat sink.

Why does Joule heating scale with I^2 while Peltier cooling scales with I?

Peltier cooling ($Q_{Peltier} = \alpha \cdot Tc \cdot I$) is linear in current because each electron carries a fixed amount of entropy determined by the Seebeck coefficient — more electrons per second means proportionally more heat carried. Joule heating ($Q_{Joule} = I^2R$) is quadratic because power dissipated by current flowing through resistance comes from electron–phonon scattering that scales with the square of current. At low current, Peltier dominates and COP improves; at high current, Joule dominates and COP collapses. The crossover is near $I/I_{max} \approx 0.25$ for typical Bi_2Te_3 — this is why the Goldilocks zone ($I/I_{max} = 0.20–0.35$) is where COP peaks.

What is the difference between material-level and module-level properties?

Material-level properties (s, ρ, k) describe a single Bi_2Te_3 thermoelectric leg or element. Module-level effective properties (α ≡ SM, R ≡ RM, K ≡ KM) describe the complete TEC module with all N couples wired in series electrically and in parallel thermally. The relationship is: $SM = 2N \cdot s$, $RM = 2N \cdot \rho / G$, $KM = 2N \cdot k \cdot G$, where G is the pellet geometry factor. The energy-balance equation $Qc = \alpha \cdot Tc \cdot I - \frac{1}{2} \cdot R \cdot I^2 - K \cdot \Delta T$ uses module-level properties. If you mistakenly use material-level values, your calculations will be off by a factor of 2N (254 for a 127-couple module).

What is the figure of merit ZT, and does a higher ZT always mean better performance?

$ZT = \alpha^2 \cdot \bar{T} / (R \cdot K)$ is a dimensionless material quality metric. Higher ZT means the material can sustain a larger ΔTmax and achieve higher COP. However, ZT peaks at a specific temperature — Bi_2Te_3 peaks near 300 K, skutterudites near 800 K. Using a material optimized for 800 K at room temperature gains nothing. For room-temperature precision cooling (0 to +85 °C), conventional Bi_2Te_3 with $ZT \approx 1$ is the correct and proven choice.

What is the difference between a TEC and a TEG?

Both use the same Bi_2Te_3 materials and the same Peltier/Seebeck physics, but in opposite directions. A TEC (cooler) uses electrical current to pump heat; a TEG (generator) uses a temperature difference to generate electricity. Modules optimized for cooling have low electrical resistance and are not optimal TEG designs. Some applications use a single module in both modes (cooling during the day, harvesting heat at night) — this is sometimes called dual-mode thermoelectric operation.

CLUSTER B — Performance and Selection

What is the maximum temperature difference a TEC can achieve?

A single-stage Bi_2Te_3 module reaches ΔTmax ≈ 65–70 °C at Th = 27 °C with zero heat load. At higher hot-side temperatures ΔTmax increases — up to ≈104 °C at Th = 125 °C (H-series only). Multi-stage (cascaded) modules can reach ΔT > 130 °C. Important: ΔTmax is measured at zero cooling load (Qc = 0) and maximum current (I = Imax). Under any real heat load, the achievable ΔT is always less than ΔTmax.

How is Qmax defined on the datasheet, and is it a practical operating point?

Qmax is the cooling power at ΔT = 0 °C and I = Imax — both surfaces at the same temperature, driven at maximum current. It is a comparison figure useful for sizing modules, not a practical operating point. At any real ΔT or any current below Imax, actual Qc will be lower. Use the normalized performance curves (Section 5.4) to find the actual Qc at your operating ΔT and chosen current.

What is the "Goldilocks zone" for TEC current, and why does it matter?

The Goldilocks zone is I/Imax = 0.20–0.35. Below this range the module pumps too little heat for its size; above it, Joule heating rises faster than Peltier pumping, COP collapses, and the module runs hot. Operating in this band maximizes COP, minimizes hot-side heat load, and extends module life to >200,000 h (under steady-state operation, proper clamping, Th ≤ 50 °C, dry environment, and limited thermal cycling). This is one of the most important practical design rules in TEC engineering.

Why should Qmax be much larger than my actual cooling load Qc?

Oversizing (Qmax >> Qc) allows the module to operate at low I/Imax, which keeps it in the high-COP Goldilocks zone. The sizing rule depends on your design priority: 1.5–2× Qc for minimum-size designs; 4–6× Qc for balanced precision; 6–8× Qc for maximum COP/lifetime (space-constrained), 4–6× Qc for balanced precision design, and 5–8× Qc for maximum COP or lifetime. Operating a barely-adequate module at high current wastes power, stresses solder joints, and shortens life. (See §5.3 for the complete design-target oversizing table.)

How do I choose between COP-Optimized, Minimum-Size, and Maximum-ΔT design methods?

The choice depends on your primary constraint. COP-Optimized (Qmax = 6–8× Qc, I/Imax = 0.15–0.25): for battery-powered devices, dense enclosures, telecom lasers. Balanced (Qmax = 4–6× Qc, I/Imax = 0.20–0.35): for most precision instruments and general lab use. Minimum-Size (Qmax = 1.5–2× Qc, I/Imax = 0.9–1.0): for TO-can packages and miniature optical receivers. Maximum-ΔT (Qmax = 10×+ Qc, I/Imax near 1.0): for IR detectors and cryogenic pre-cooling. See Section 6.5 for detailed walkthroughs.

How do I select the right TEC module for my application?

Follow the five-step process in Section 7: (1) determine the real heat load Qc, (2) determine the required ΔT, (3) choose the Qmax/Qc ratio based on design target, (4) check the ATE1-127 series selection guide for footprint and current/voltage limits, and (5) verify the operating point stays in the Goldilocks zone (I/Imax ≈ 0.20–0.35). Use the ATI TEC Design Calculator at www.analogtechnologies.com/tec-calculator for automated iteration.

What is the "negative-ΔT" regime, and how can COP exceed 10?

The negative-ΔT regime occurs when the TEC cold side is warmer than the hot side (Tc > Th, so ΔT < 0). The TEC acts as an "active heat spreader" — pumping heat in the same direction it would naturally flow, but accelerating the process. COP can exceed 10 (even 15–20 for very small |ΔT|) because the required current is very low. Example: in Section 9.3 (AI accelerator hotspot cooling), a TEC operating with ΔT = −2.3 °C achieved COP = 14.4 with only 2.8 W of input power moving 40 W of hotspot heat.

Why does ΔTmax increase with hot-side temperature?

ΔTmax increases with Th because Peltier cooling scales with the cold-side absolute temperature: $\Delta T_{max} = \frac{1}{2} \cdot Z \cdot T_c^2$. At Th = 27 °C, ΔTmax ≈ 66 °C; at Th = 50 °C, ΔTmax ≈ 76 °C; at Th = 100 °C, ΔTmax ≈ 94 °C. Warmer ambient means a warmer cold side at the maximum-ΔT condition, so each electron carries more heat per trip. But standard S-series modules use BiSn solder (138 °C melting point) and cannot sustain Th > 85 °C — use H-series (SnSb solder, 232 °C) for elevated temperatures.

CLUSTER C — Thermal Design and Heat Management

How do I calculate the correct heat-sink size?

Size the heat sink for Qh, not Qc. Qh = Qc + Pin (all heat rejected at the hot side includes both the load you are removing AND the electrical power consumed by the TEC). The required thermal resistance is Rhs,max = (Th − Tamb) / Qh. Underestimating Qh is the single most common cause of a TEC system that cools poorly under full load. A heat sink sized only for Qc will overheat under load, raising Th and reducing the achievable ΔT.

How does TIM (thermal interface material) thickness affect performance?

Every 25 µm of thermal paste adds approximately 0.05–0.10 K/W of thermal resistance per cm² of contact area. Recommended thickness is 50–100 µm — thin enough to minimize resistance, thick enough to fill surface imperfections. Too much paste (>150 µm) acts as a thermal insulator; too little leaves air gaps. Apply a thin, uniform layer and use moderate clamping pressure (1.0–2.0 MPa) to achieve optimal bond-line thickness.

How do I prevent condensation on my TEC cold side?

When Tc is at or below the local dew point, moisture will condense and cause corrosion, electrical shorts, and accelerated mechanical fatigue. Use a sealed (S) module, seal all edges of the cold plate with silicone RTV, purge the enclosure with dry nitrogen or desiccant, and ensure that any thermally conductive paths to the cold side are interrupted or sealed at the dew-point isotherm.

Do I need a different heat sink for heating vs. cooling mode?

Size the heat sink for the cooling mode condition (larger Qh). In cooling mode, Qh = Qc + Pin. In heating mode, only Pin is rejected to the heat sink (the useful heat goes to the device). The heat sink sees less heat in heating mode, so if it handles cooling mode, heating mode is automatically covered.

Does altitude or air pressure affect TEC performance?

The TEC module itself (solid-state, no gas) is unaffected by altitude. However, forced-air and natural-convection heat sinks perform worse at altitude because lower air density reduces convective heat transfer. At high altitude or in vacuum, switch to a liquid cold plate or conduction cooling for the hot side, and recheck the heat-sink thermal resistance budget accordingly.

Can I stack multiple TEC modules for deeper cooling?

Yes — this is called cascaded or multi-stage TEC cooling. Each stage pumps heat to the next stage's hot side. Two-stage: ΔT ≈ 80–100 °C; three-stage: ΔT ≈ 110–130 °C. Each additional stage reduces overall COP dramatically and increases complexity. Use cascading only when ΔT > 80 °C is the primary requirement and efficiency is secondary. Contact ATI for custom multi-stage assemblies.

CLUSTER D — Controller and Electrical Drive

Why do I need a dedicated TEC controller?

A TEC requires precise, low-ripple, bidirectional DC current with closed-loop temperature feedback. A bare power supply cannot maintain stable temperature — it provides constant voltage, not constant temperature. A dedicated controller (such as the ATI TEC series) provides PID-controlled current with <0.1% ripple, bidirectional operation for both heating and cooling, and thermistor feedback for ±0.002 °C stability.

Can I drive a TEC directly from a microcontroller PWM pin or an H-bridge?

An H-bridge can deliver bidirectional current and is acceptable for non-precision applications, but PWM ripple reduces effective cooling capacity (every ripple cycle adds I^2R heat without contributing to Peltier cooling) and degrades setpoint stability. For precision temperature control (laser diodes, optical sensors, analytical instruments), always use a dedicated linear TEC controller with <0.1% current ripple such as the ATI TEC series.

How much current ripple is acceptable?

General cooling: <10%. Precision temperature control: <5%. Laser diode wavelength stability: <2%. Ultra-precision (millikelvin): <1%. Ripple adds extra Joule heating without contributing to Peltier cooling, reducing net capacity and degrading stability. ATI linear controllers deliver ripple below 0.1% with no output LC filter required.

Can I connect multiple TEC modules in series or parallel?

Yes. Wiring in series increases the total drive voltage while keeping current constant — useful when your controller has a higher voltage rating than a single module requires. Wiring in parallel splits the current between modules at the same voltage. Never mix series/parallel stacks with modules of differing Imax or Vmax ratings, as current imbalance will degrade performance and reduce life.

How does a TEC behave in heating mode?

When you reverse the current, the heat-pumping direction reverses. In heating mode, the device receives Qheat = Qc + Pin — both the Peltier-pumped heat AND the Joule heat arrive at the target. Heating COP = COPcooling + 1, which is always > 1. This makes TECs exceptionally efficient for precise temperature control near ambient — you can heat with >100% efficiency relative to input

power. Sign convention: all equations in this paper assume cooling mode (positive current = cold side absorbs Qc); reverse polarity for heating.

What causes oscillation in my TEC control loop?

Common causes: (1) PID gains too aggressive for the actual thermal time constant (τ = C/Ktotal, typically 10–60 s for a TEC assembly); (2) thermistor mounted far from the load, introducing transport delay; (3) PWM drive coupling noise into the temperature signal; (4) heat-sink thermal resistance varying with fan speed or ambient. Start with conservative gains (integral time = 3–5× the thermal time constant) and tighten gradually.

CLUSTER E — Mounting, Thermistor, and Assembly

What thermistor should I use with an ATI TEC controller?

Use an NTC (negative temperature coefficient) thermistor with a nominal resistance of 10 kΩ at 25 °C and β ≈ 3977 K — the value all ATI PID controllers are calibrated for. Mount it within 5 mm of the controlled surface and thermally couple it with a small dab of thermal grease or epoxy. A mismatched or loosely mounted thermistor is a common source of setpoint error and oscillation.

Where should I place the thermistor for accurate temperature control?

Mount on the cold plate (NOT on the TEC ceramic surface), as close to the thermal load as possible (≤5 mm). Mounting on the TEC ceramic puts the TIM resistance between the measurement point and the actual load, producing an uncontrolled temperature offset that varies with heat load and paste thickness. Use thermal paste between thermistor and cold plate. Electrically insulate the thermistor if the cold plate is metallic. For ultra-precision applications, use a four-wire connection to eliminate lead-resistance drift.

How do I calculate the correct mounting torque?

Target compression pressure of 1.0–2.0 MPa distributed evenly across the module face. For a 40×40 mm module with four M3 lubricated screws: T = (C × D × P × A) / N = (0.15 × 0.003 × 1,000,000 × 0.0016) / 4 ≈ 0.18 N·m. Critical warnings: excessive torque causes substrate bowing and air gaps; reduce torque if mating surfaces are thin (copper <3.2 mm, aluminum <6.4 mm); never apply shear force — Bi_2Te_3 pellets are brittle.

What temperature stability can I realistically expect?

A well-designed system using a linear-drive ATI controller, a properly sized module, and a securely bonded thermistor can achieve ±0.002 °C steady-state stability under constant load. Instability is usually caused by PID gains not tuned for the actual thermal time constant, a thermistor mounted far from the load, or PWM-drive ripple coupling into the temperature signal.

How do I detect a failed or drifting thermistor?

Cross-check by adding a redundant temperature sensor and comparing readings. A healthy NTC thermistor drifts less than 0.02 °C per year; readings that disagree by more than 0.1 °C at the same setpoint indicate drift. Replace both with calibrated units if the cross-check fails. ATI 10 kΩ NTCs are interchangeable to ±0.1 °C, so drop-in replacement does not require recalibration.

CLUSTER F — Reliability, Aging, and Troubleshooting

Why is my TEC not cooling enough?

Top causes, in diagnostic order: (1) Undersized heat sink — must handle Qh = Qc + Pin, not Qc alone. (2) Operating current too high — use I/Imax = 0.20–0.35 for best COP. (3) Excess thermal paste — keep to 50–100 µm. (4) Reversed polarity — cold and hot sides are swapped. (5) Air gaps in the thermal stack — verify flatness and clamping. (6) Thermistor not on the cold plate — controller is regulating the wrong temperature. Check these in order; the first three account for >80% of field complaints.

How can I tell if my TEC module is degrading?

Monitor the AC resistance at 1 kHz (RAC) with a low-voltage LCR meter. A new module matches the datasheet value within ±5%. Warning thresholds: <5% = normal; 5–10% = early warning, schedule inspection; 10–20% = degradation confirmed, plan replacement; >20% = end-of-life, replace immediately. DC resistance is unreliable for health monitoring because it varies with temperature and contact resistance.

What is a realistic MTBF for an ATE1-127 module?

For steady-state operation at Th ≤ 50 °C and I ≤ 0.35·Imax, expect 200,000+ hours (>22 years) MTBF. For moderate cycling (ΔT swings <40 °C, fewer than one per hour), 100,000+ cycles before solder fatigue becomes likely. For aggressive cycling (PCR-style, 60 °C swings at 5+ per hour), 10,000–50,000 cycles. The dominant wear-out mechanism is thermo-mechanical fatigue at solder interfaces.

What causes a TEC module to crack or fail early?

Dominant failure mechanisms: (1) Thermal cycling fatigue — CTE mismatch between Bi_2Te_3 pellets and ceramic substrate accumulates stress with each cycle. (2) Excessive mounting torque — the ceramic substrate is brittle and will crack above 5 N·cm. (3) Moisture ingress in non-sealed modules operating below dew point. (4) Operating at I > Imax for extended periods, which melts solder bonds. Staying in the Goldilocks zone (I/Imax ≤ 0.35) and using a sealed variant in humid environments are the two highest-impact reliability choices.

Can I operate a TEC in a vacuum?

Yes, and it works better than in air because the parasitic convective heat leak is eliminated. The trade-off is that all heat must leave the hot side by conduction or radiation alone — vacuum operation typically requires a high-conductivity copper or aluminum heat-sink path to a chamber wall. Sealed (S) modules are recommended because vacuum will outgas moisture trapped in unsealed modules.

Is the TEC sensitive to ESD?

Less so than a typical CMOS chip — the Bi_2Te_3 pellets and copper interconnects can absorb static discharges that would destroy a transistor. However, the leads can carry static onto the connected controller, which IS ESD-sensitive. Standard ESD precautions apply when handling before mounting: grounded wrist strap, anti-static work surface, ESD-rated bags. After mounting and wiring to a controller with ESD protection, the TEC needs no special handling.

CLUSTER G — Applications and Commercial

Can TECs be used for AI chip cooling?

Yes — and this is one of the fastest-growing TEC applications. Modern AI accelerators (GPUs, TPUs, FPGAs) create intense thermal hotspots that conventional heat sinks cannot eliminate. A TEC operating in the negative-ΔT regime (active heat spreading) can move 40+ W of hotspot heat with only 2–3 W of input power at COP > 10. This does not replace the main cooling system — it supplements it by eliminating the thermal gradient between the hotspot and the heat spreader. See Example C in Section 9.3. For sub-ambient cooling, first-pass practical COP is usually 0.3–3 depending on ΔT and current ratio.

When should I use the H-series (high-temperature) instead of standard?

Use the H-series whenever the hot-side temperature (Th) may exceed 85 °C under worst-case conditions. Standard modules use BiSn solder (138 °C melting point) and suffer accelerated creep above 85 °C. H-series modules use SnSb solder (232 °C melting point) and can sustain Th up to 200 °C. Applications: automotive under-hood, industrial process control near furnaces, high-power modules with marginal heat sinks, and any system where Th may exceed 85 °C under any condition.

What about sealed vs. unsealed modules?

Sealed (S) modules have the edges potted with silicone or epoxy to prevent moisture ingress. Use sealed modules whenever: (1) Tc may drop below the local dew point, (2) the environment is humid (>60% RH), (3) the application is outdoors or in a non-climate-controlled space, or (4) long life (>5 years) is required. Unsealed modules are acceptable only for dry laboratory environments with Tc always above dew point.

Can a TEC be used to generate electricity (as a TEG)?

Yes. Applying a temperature difference generates a voltage via the Seebeck effect. However, modules optimized for cooling are not optimal TEG designs — dedicated thermoelectric generator modules use different pellet geometry and doping. For small energy-harvesting experiments a TEC module works fine; for production TEG systems, use modules specifically characterized for power generation.

Can I use a TEC to cool a battery or energy storage system?

Yes, with caveats. TECs are excellent for precision battery thermal management (±1 °C uniformity) in small packs, but their COP at large heat loads can be low. For large battery systems (>1 kW cooling), vapor-compression or liquid cooling is more energy-efficient. TECs shine in small-format precision applications — reference cell conditioning, battery characterization equipment, and drone battery pre-conditioning.

What is the typical lead time for ATE1-127 modules? [availability subject to change]

Stocked variants (ATE1-127-3AS, -5AS, -8AS, -10AS, all sealed, standard solder) ship within 1–2 business days from ATI's California warehouse. High-temperature (H) variants and tolerance-lapped versions have 2–4 week lead times. For production volumes (>1000 units), schedule with

sales 8–12 weeks ahead. Single-unit evaluation pricing is available through shop.analogtechnologies.com. [availability subject to change]

Does ATI offer system-level design support?

Yes. The applications engineering team supports module selection, controller configuration, custom heat-sink design, thermal simulation, and production validation. For complex multi-stage or high-power-density applications, ATI can model the complete thermal loop and recommend the optimal module/controller/sink combination. Contact sales@analogtechnologies.com or visit www.analogtechnologies.com.

For additional technical support, visit www.analogtechnologies.com or contact our engineering team at sales@analogtechnologies.com.

Can I use a TEC without a heat sink?

No for continuous cooling. A TEC does not destroy heat; it pumps heat to the hot side and adds its own electrical input power. The hot side must reject Qh = Qc + Pin to ambient or a liquid loop. Without a heat sink, the hot side quickly warms up, ΔT collapses, and the cold side may become warm or even hot.

Why does my TEC get hot on both sides?

Usually the heat sink is undersized, the module is driven too hard, the polarity is reversed, or the cold-side load exceeds the module's capacity. Verify polarity, reduce current, improve the heat sink, and calculate Qh = Qc + Pin to confirm the hot side can reject the total heat.

Should I choose a sealed TEC module?

Choose a sealed module when the cold side may operate below the dew point or when the environment is humid. The perimeter seal helps reduce moisture ingress and condensation-related corrosion, but it does not eliminate the need for system-level condensation control (insulation, desiccant, dry-gas purge, or hermetic enclosure).

Can I stack (cascade) TECs for larger ΔT?

Yes, but only when a single-stage module cannot meet the required ΔT. Cascaded TECs can achieve larger temperature spans (up to 100–130 °C with two or three stages), but efficiency drops sharply because each upper stage must pump the load plus the electrical heat from the lower stage. Use multi-stage modules only after verifying the heat-sink capacity and total power dissipation.

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