TEC CONTROLLER EVALUATION KIT TECEV103

(updated 06/17/04)

Our TEC controller modules can be evaluated conveniently by using this evaluation kit TECEV103 which comes with an evaluation board, TECEVB103 and a TEC controller module of TEC -A1 (there is no internal compensation network in side). The main purpose of using the evaluation board is to tune the compensation network on the board for match ing the characteristics of users' thermal load. The objectives of the tuning are to minimize the response time of the thermal control loop and the dynamic temperature tracking errors, while keeping the control loop stable.

1. Connection

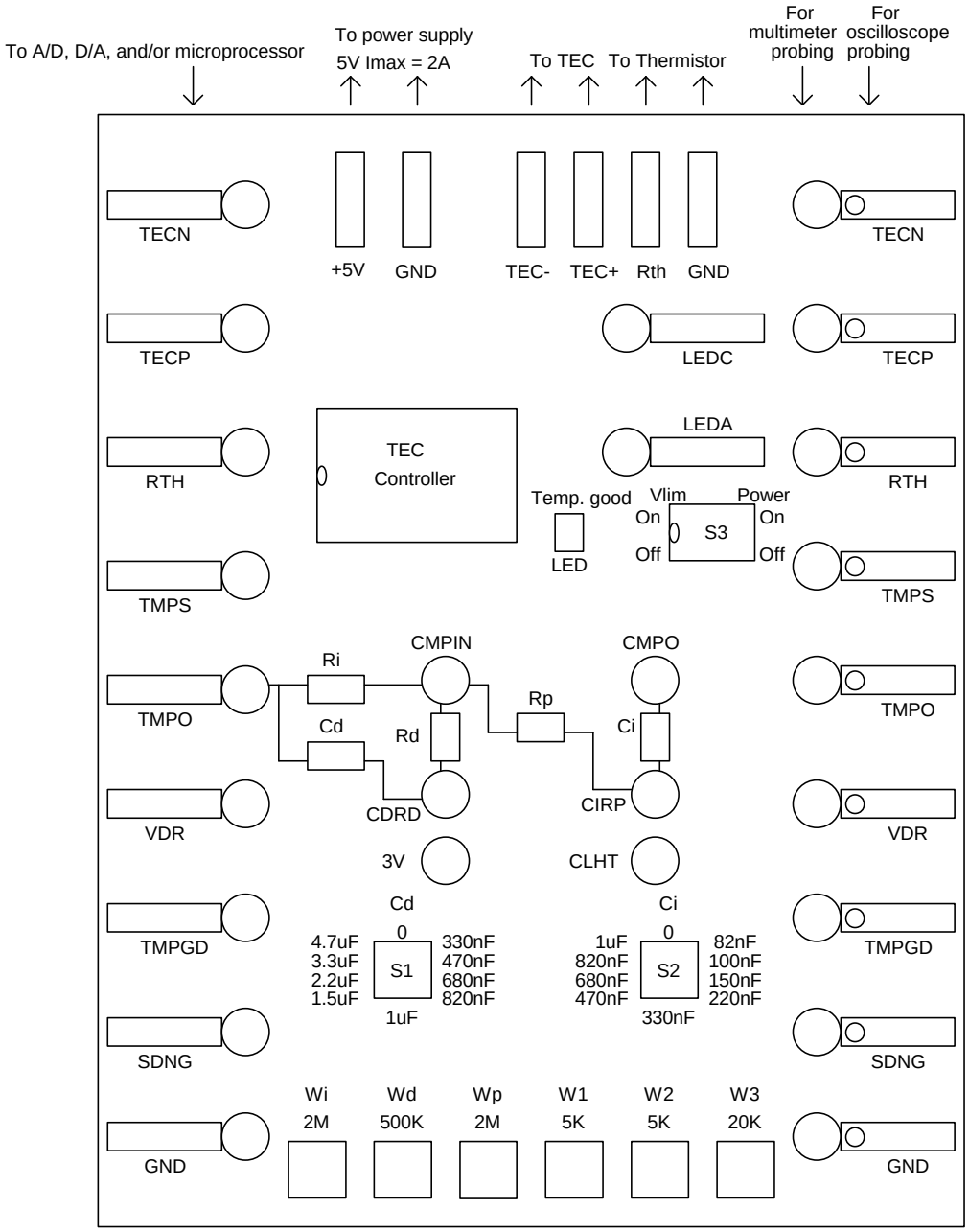

Figure 1 TEC Controller Evaluation Board TECEV103

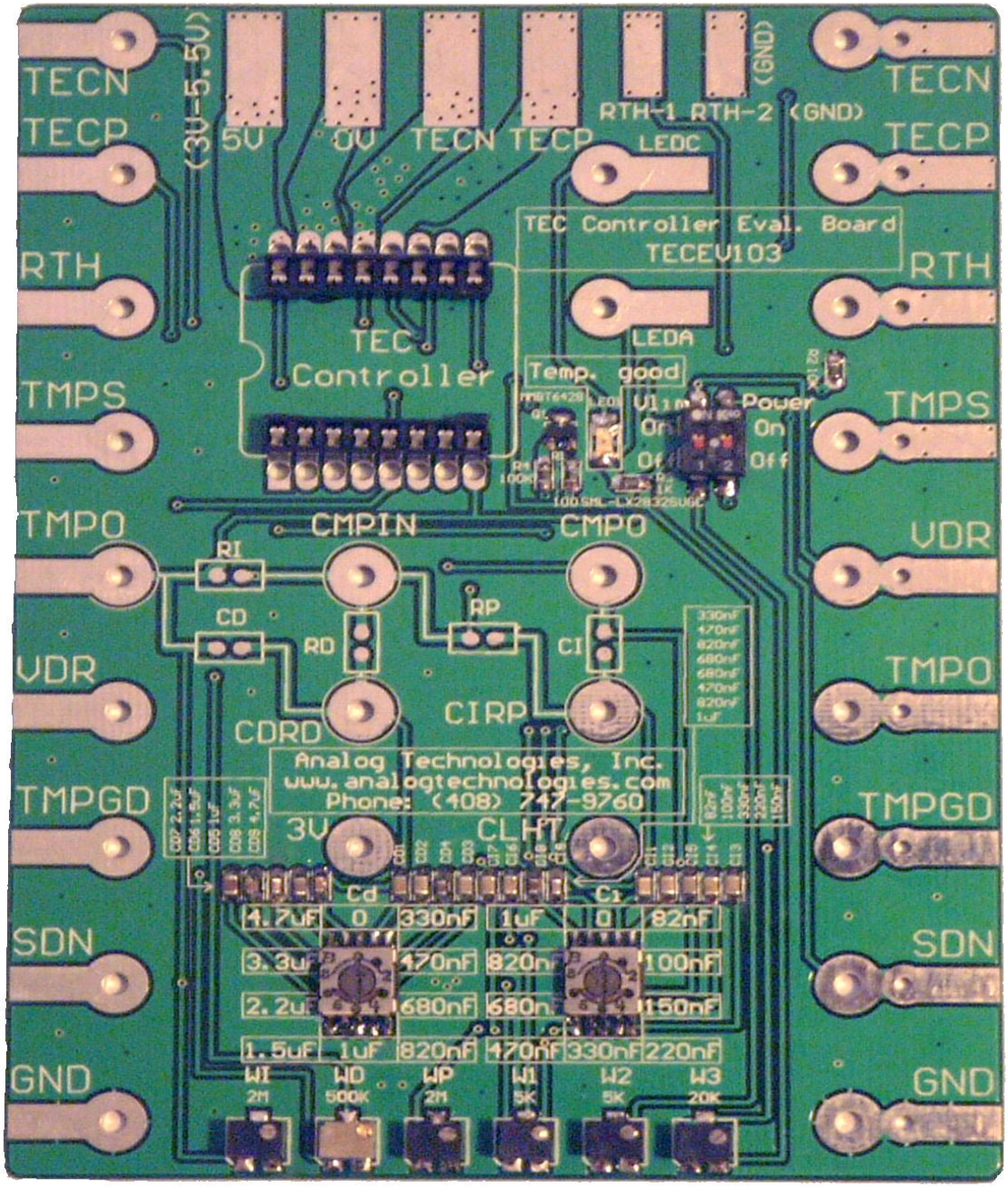

Figure 2 TECEV103 Photo

Figure 1 shows the layout of the evaluation board and Figure 2 shows its photo.

These are the procedures for the adjustment.

1. Set up basic connections. Connect a 5V DC power supply and the TEC terminals in the right polarity as indicated onto the board. Connect the thermistor terminals to the board, there is no polarity requirement. Turn the two switches, for Vlim and Power, to the off positions (down side). Check the evaluation board connections, making sure that they are all correctly connected. Turn on the Power side switch and see how the Controller works.
2. Tune the compensation network. The purpose for this step is to match the controller compensation network with the thermal load characteristics thus that the response time and temperature tracking error are minimized. Adjust the potentiometer W1 to ch ange

the set-point temperature TMPS just a small amount, simulating a step function . At the same time, connect an oscilloscope at the VDR test pin (on the right side of the evaluation board), set it to a scrolling mode (0.2 Second/Division or slower) and monitor the waveform of VDR as TMPS is fed by a step function signal . The circuit in the compensation network is shown in Figure 3 below.

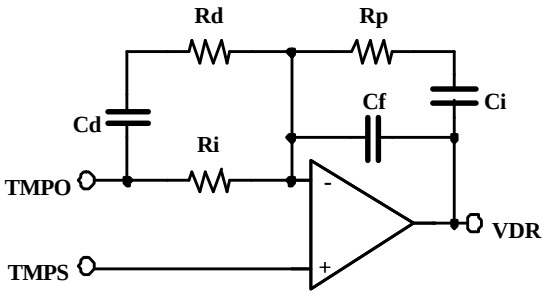

Figure 3 Compensation network

The transfer function of the compensation network, defined as H(ω)=VDR(ω)/TMPO(ω), is shown in figure 4.

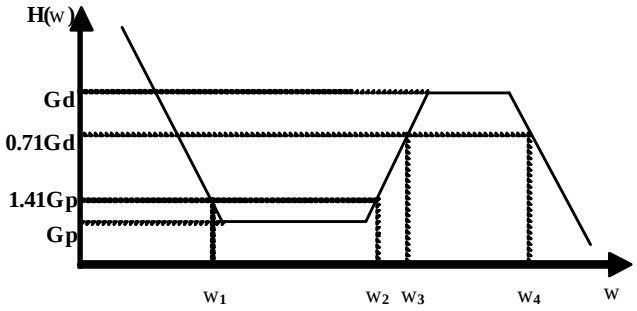

Figure 4 Transfer Function of the Compensation Network

In principle, these are the impacts of the components to the tuning results:

a. Rp/Ri determines the gain for the proportional component of the feedback signal which is from the thermistor, Gp = Rp/Ri, in the control loop, the higher the gain, the smaller the short term error in the target temperature (which is of the cold side of the TEC) compared with the set-point temperature, but the higher the tendency of the loop's instability.

b. Rp/Rd determines the gain for the differential component, Gd = Rp/(Rd//Ri) ≈ Rp/Rd, where symbol "//" stands for two resistors in parallel, since Ri >> Rd, Rd//Ri = Rd. The higher the gain, the shorter the rise time of the response, the more the overshoot and/or the undershoot will be.

c. Ci*Rp determines the corner frequency , ω_1= 1/(Ci*Rp), where the integral component starts picking up, as the frequency goes down. It determines the cut-off frequency be low which the TEC controller will start having a large open loop gain. The higher the open loop gain, the smaller the tracking error will be.

d. Cd*Ri determines the corner frequency , ω_2=1/(Cd*Ri), where the differential component starts picking up (see Figure 4), as the frequency goes up.

e. Cd*Rd determines the corner frequency, ω_3=1/(Cd*Rd), where the differential component starts getting flat. It determines the cut-off frequency above which the TEC controller will give extra weight or gain in response.

f. Cf*Rp determines the corner frequency , ω_4=1/(Cf*Rp), where the differential component starts rolling down . Since this frequency is way higher than being needed for controlling the TEC, ω_4 does not need to be tuned. The capacitor is built into the TEC controller module, not the evaluation board.

To start the tuning, turn off the differential circuit by setting Cd Open. Turn W1 quickly by a small angle, back and forth, approximately 5 seconds per change. Set Ci to 1uF, set Ri to 1M, and increase the ratio of Rp/Ri as much as possible, provided the loop is stable, i.e. there are no oscillations seen in VDR. Then, minimize Ci as much as possible, provided the loop is stable. The next step is to minimize Rd and maximize Cd while maintaining about 10% overshoot found in VDR. Optimum result can be obtained after diligent and patient tuning. The tuning is fun and important.

When the TEC controller is used for driving a TEC to stabilize the temperature of a diode laser, there is no need to turn on the laser diode while tuning the TEC controller. To simulate the active thermal load given by the laser diode, setting the set-point temperature lower than the room temperature is enough.

For a typical laser head used in EDFA's or laser transmitters (found in DWDM applications, for instance), Ri = 1MΩ, Rp = 1MΩ, Ci = 680nF, Cd = 1.5μF, and Rd = 250kΩ. These values may vary, depending on the characteristics of a particular thermal load.

To be conservative in stability, use larger Ci and larger Ri; To have quicker response, use smaller Rd and larger Cd.

The closer to the TEC the thermistor is mounted, the easier to have the loop stabilized, the shorter the rise time and the settling time of the response will be.

3. After tuning, the values of the capacitors for Cd and Ci can be read off the capacitor selection switches. The values of the resistors, Ri, Rd and Rp, can be measured by an Ohm-meter by connecting to the resistor pins. As seen in the photo of Figure 2, Ri can be read off between TMPO and CMPIN test points; Rd can be read off

between CMPIN and CDRD test points; Rp can be read off between CMPIN and CIRP test points.

4. After the compensation network is tuned properly, we can now adjust set-point temperature to see if the TEC controller can drive the target temperature to a certain range and with high stability . Turn the temperature set-point TMPS potentiometer W1 while monitoring its output voltage at TMPS test point (4th row on either left or right side of the board), watch the LED: when it turns to green, the target temperature is locked to the set-point temperature within 0.1 °C or less. The relationship between the set-point voltage vs. the set-point temperature is given in the datasheet. After seeing the LED lock into the set-point temperature, VDR should be a constant voltage as shown in the oscilloscope and the voltage between TMPS and TMPO should be very small, less than 10mV. When a standard TEC controller is used, the 10mV represent a 0.07° temperature error.
5. Set output voltage limit.
6. To know more parameters of the TEC controller.

a. To know the actual target temperature, use a voltage meter to measure the voltage between the TMPO and the GND pins, the reading result is: target temperature = 15 °C + (TMPO voltage (V))*6.67 °C for approximation (see the curve in the TEC controller data sheet).

b. To know how hard the TEC is working, measure the voltage VDR by a voltage meter or an ADC, TEC voltage = 2.5V – VDR. When the TEC voltage (from the calculation) is positive, it is in cooling mode; when the TEC voltage is negative, it is in heating mode. Cool/ Heat Balance CLHT can be adjusted by W2. TEC maximum voltage can be reduced by reducing W3, make sure Vlim switch is now turned to the on position.

c. To try other values of capacitors not provided by the evaluation board for the capacitors in the compensation network, turn the capacitor switches you want to try to the top point, the "0" position, connect the component to the corresponding soldering pads as marked on the evaluation board.

d. To shut down the TEC controller, turn the Power switch to the "Off" position, see Figure 2.

e. To control the set-point temperature directly by using a DAC, set the set-point temperature POT W1 to the middle point (25 °C), on which the TMPS is about 1.5V, the half value of the reference voltage, connect TMPS test point to the output of the DAC and use this formula for approximation when the input voltage is between 0V and 3V:
set-point temperature (°C) = 15 °C + (TMPO voltage (V))*6.67°C. The maximum voltage allowed is Vps (power supply). See the curve in the TEC controller data sheet.

f. To control the TEC voltage directly by using a DAC, connect VDR to the output of the DAC and use this formula: TEC voltage = 2.5V – VDR (V).

g. To shut down the TEC controller by using a microprocessor, turn off the Power switch, connect SDN test point (2nd row from the bottom side, on both left and right columes.) to one of its digital outputs. When pulling low, the TEC controller is shut off. When pulling high SDN, the TEC controller is turned on.

h. The evaluation schematic is given in Figure 5.

Using the TEC controller for more applications not described here, and/or having any questions, please free to contact us.

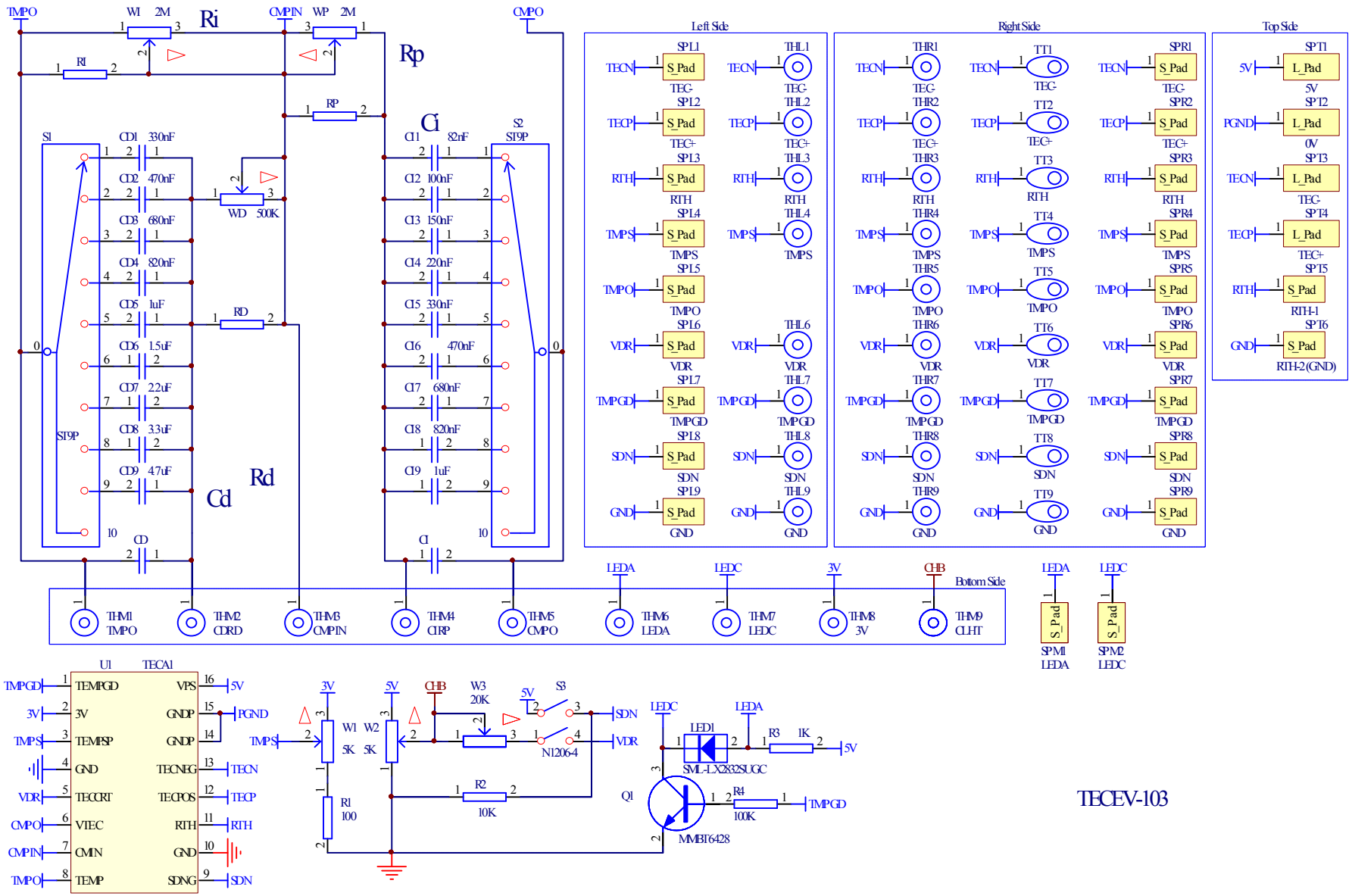

Figure 5 Evaluation Board Schematic